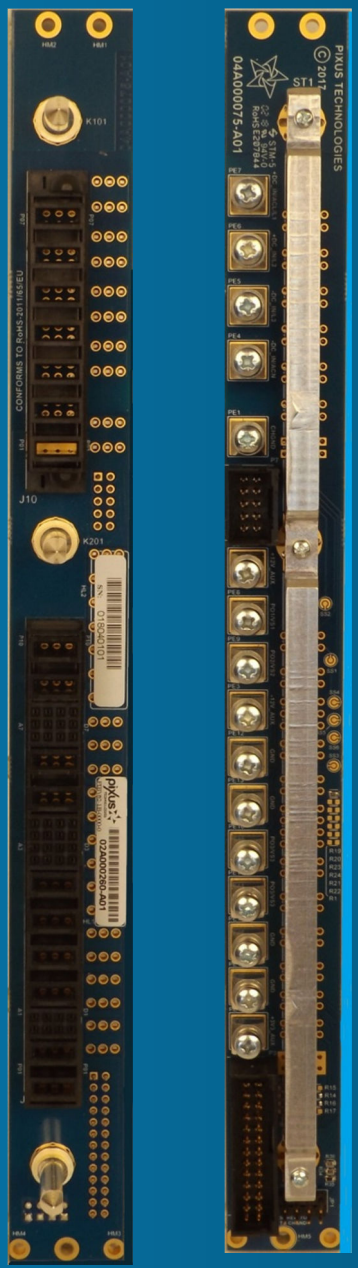


USER GUIDE

3U/6U VITA 62 PSU

Contacting Us

Pixus Technologies Inc.,
50 Bathurst Drive, Unit 6
Waterloo, Ontario
Canada
N2V 2C5

(519) 885-5775

Visit our home page at www.pixustechnologies.com for more information about Pixus products and services.

Issue	Date	Description
1.0	10-May-2018	Product release

TYPOGRAPHICAL CONVENTIONS USED IN THIS DOCUMENT

Items	Convention
You will see the following icons periodically throughout this manual:	
	The **WARNING** icon cautions you against an action or treatment that could threaten the responsiveness of the equipment or the integrity of your current work.
	The **INSPECT** icon alerts the reader to follow inspection instructions to ensure product is not damaged and in operational order.
	The **NOTE** icon notifies you of the information that makes a procedure easier or clarifies an earlier description.
Headings, titles, sections or words of importance.	These items appear in **bold** typeface. Example: **Any changes or modifications…….**
Variable placeholders, references to other documents, new or special terminology, and emphasis.	These items appear in *italic* typeface. Example: *Table 3-1*, displays……
References to chapters and sections of documents, and citations of messages displayed to users.	These items appear in “quotation marks.” Example: For more information, refer to “Connections”, section 3….

Revision History

Revision	Date	Description	Author
1.0	10-May-2018	Released for product approvals	

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

SECTION ONE

1. INTRODUCTION

This section provides a brief overview about Pixus Technologies Inc. This section describes the following:

- 1.1 Pixus Technologies Inc.
- 1.2 Contact Information
- 1.3 Background Information
- 1.4 Applicability

1.1. PIXUS TECHNOLOGIES INC.

Pixus Technologies specializes in the design and manufacture of electronic packaging solutions for the global embedded computer market. The company is comprised of three business units: Backplanes, Enclosure & System Solutions and Components.

Leveraging over 20 years of innovative product development, Pixus Technologies' embedded backplanes and systems are focused primarily on xTCA, OpenVPX, CompactPCI, PCIe and custom designs. The company offers unsurpassed thermal management solutions, creative design innovations, and backplane design expertise. Pixus also offers modular 19" rackmount enclosure solutions and instrument cases to a wide range of industries, as well as precision components such as front panels, handles, and card guides.

The approach to each customer requirement is a simple consultative philosophy - understand the specific program requirements and create the best solution that meets the time frame, architecture, technology and cost objectives.

1.2. CONTACT INFORMATION

For questions about the Pixus product or about Pixus in general, please contact us using the following information:

Phone Number:	(519) 885-5775
Fax Number:	(226) 444-0225
Web Address:	www.pixustechnologies.com
Mailing Address:	Pixus Technologies Inc. 50 Bathurst Drive, Unit 6 Waterloo, Ontario Canada N2V 2C5

For Pixus product support, see the Pixus web site: www.pixustechnologies.com

1.3. BACKGROUND INFORMATION

When designing VPX® systems, use the following documents for reference:

- ANSI/VITA® 62.0 Modular Power Supply Standard
- ANSI/VITA® 48.0 Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)
- ANSI/VITA® 48.1 Mechanical Specification for Microcomputers Using REDI Air Cooling
- ANSI/VITA® 46.0-2007 ANS for VPX Baseline Standard
- ANSI/VITA® 46.10 Rear Transition Module for VPX
- ANSI/VITA® 46.9 PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard
- ANSI/VITA® 65.0-2017 OpenVPX System Standard
- ANSI/VITA® 65.1-2017 Open VPX System Standard – Profile Tables
- IEEE Std. 1101.1-1998
- IEEE Std. 1101.10-1996
- IEEE Std. 1101.11-1998
- RoHS 2002/95/EC

1.4. APPLICABILITY

This User Guide is applicable to the following model(s):

Model	Description
PIBV62-1B-0000-0	Backplane Power VITA 62 6Ux5HP
PIBV62-2B-0000-0	Backplane Power VITA 62 3Ux7HP

Table 1-1: Applicability

SECTION TWO

2. FEATURES

The Power Interface Boards (PIBs) have been designed with the following features:

- 3Ux7HP or 6Ux5HP wide backplane supporting one VITA 62 power supply slot.
- Two ½U breakaway sections for chassis airflow management.
- One stiffener on the 6U for added rigidity.
- ANSI/VITA® 62.0 compliant.
- Configurable remote or local voltage rail sensing.
- Power elements for primary power entry.
- Power elements and/or spade lug terminals (3U only) for secondary power access.
- Various connectors for access to signals.

Figure 2-1 through Figure 2-2 illustrate the major features of the backplanes, showing approximate locations for all connectors. Objects drawn as solid lines are on the front side of the backplane. Objects drawn as dashed lines are on the rear. Shaded objects are on both sides.

Figure 2-1 on page 9 illustrates the PIBV62-2B-0000-0 backplane.

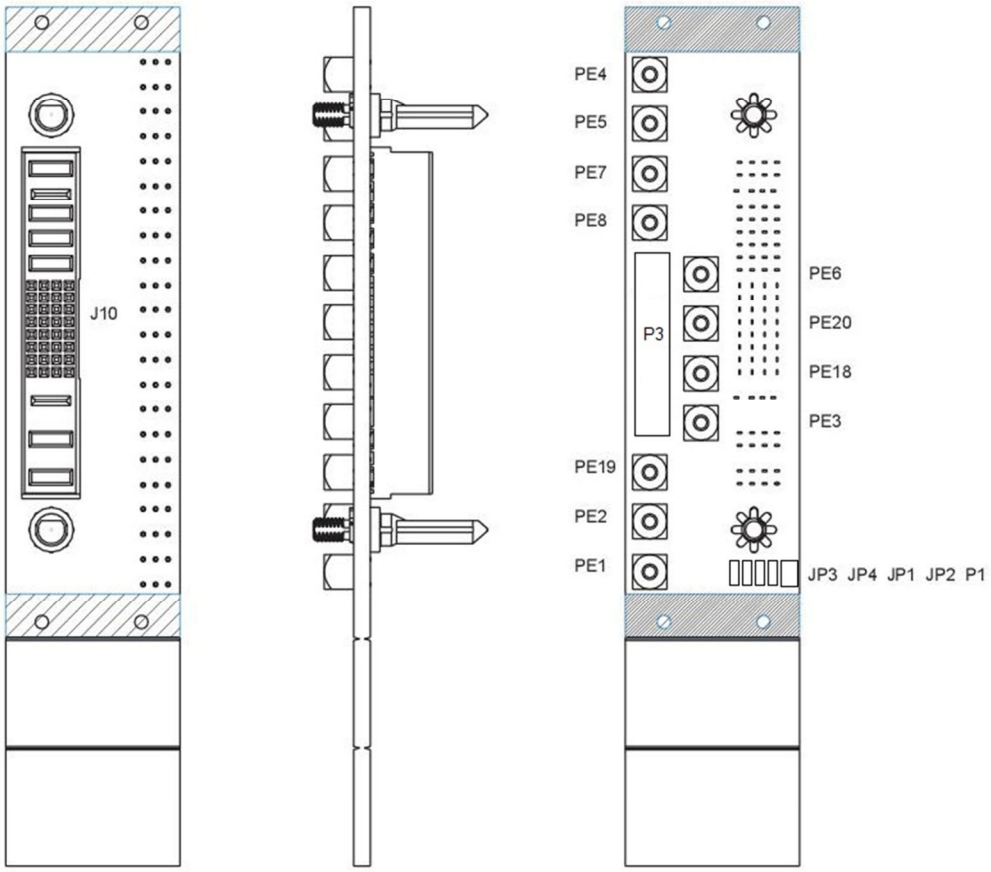


Figure 2-1: PIBV62-2B-0000-0 PIB

Figure 2-2 on page 10 illustrates the PIBV62-1B-0000-0 backplane.

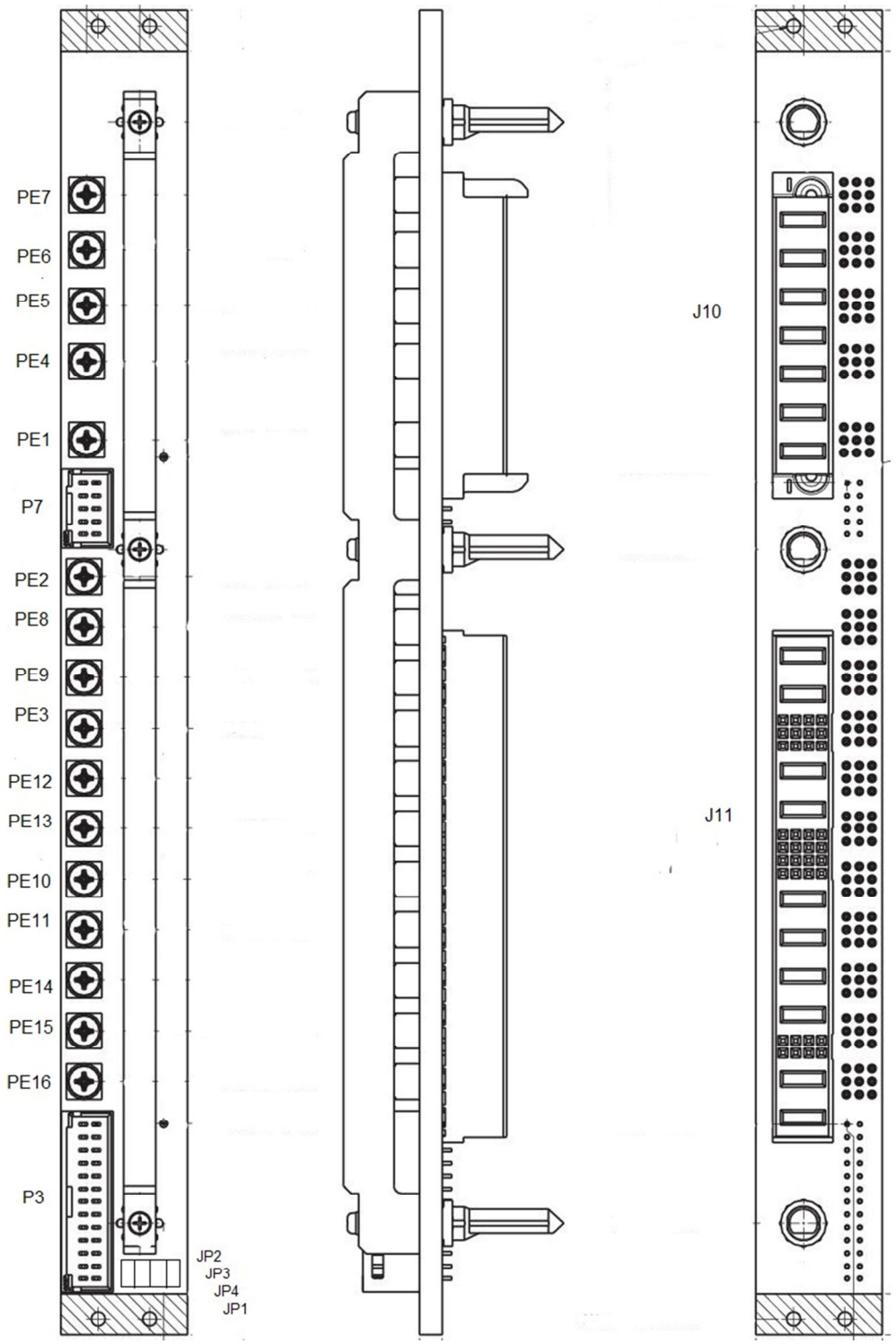


Figure 2-2: PIBV62-2B-0000-0 PIB

SECTION THREE

3. QUICK START

The PIBs comply with the VITA 62 standard as it was when the Backplanes were created.

This chapter will provide an overview of basic operating procedures, including the following:

- Inspecting Your Backplane
- Installing Your Backplane In A Subrack
- Powering Your Backplane

3.1. INSPECTING YOUR BACKPLANE

Take great care when handling the backplane. Improper handling could cause damage to the connector pins.
Always handle the backplane from the edges, never the connectors.

The first item that must be done before starting to utilize your backplane is to perform a thorough inspection.

During the course of handling, shipping and assembly, pins, mounting screws and other items could become damaged and/or loose. Operating a damaged backplane could cause serious damage to the backplane and/or devices that interface to it.

Take a few minutes to visually inspect that all of the connector pins are straight, screws are tight, etc.

Repair any bent pins, loose screws, etc. before proceeding. If damage to the backplane is deemed too extensive, call Pixus Customer Service for assistance on how to proceed.

3.2. INSTALLING YOUR BACKPLANE IN A SUBRACK

The PIBs mount into a sub-rack using M2.5 screws along the rows of mounting holes situated at the top and bottom end of each slot, with all mounting holes connecting to chassis ground with the exception of one.

The mounting rail areas of the backplane have exposed strips of copper that are connected directly to the chassis ground of the backplane.

The backplane must be mounted in the sub-rack with insulator strips between it and the rails. Applications where conductive strips are utilized must be inspected to make sure there is no electrical contact between the rails and any device on the backplane.

As stated above, there is one mounting screw that allows digital ground to be tied to chassis (frame) ground. The mounting hole that connects to digital ground is marked with the corresponding symbol (⏚) on the bottom silkscreen.

The arrow in Figure 3-1 on page 12 illustrates the screw location (HM5) for the single ground tie point.

Refer to the subrack user guide for information on torque limits for the mounting screws.

When installing the optional stiffener (part# 83A000379-A##), you must locate these where shown in Figure 2-2 on page 10. Note that the stiffener is not symmetrical and as such, will only fit properly in one direction.

Figure 3-1: Digital Ground – Chassis Ground Tie Point

3.3. POWERING YOUR BACKPLANE

AC/DC and chassis ground inputs to the PIB is done with M3 power elements.

The power elements and backplane are capable of sinking 60A when derated for a 30°C temperature rise.

3.3.1. 3U POWER

Table 3-1 on page 12 defines the relationship between the power elements and power rails.

Power Element	J10 Pin #	Voltage
PE1	P1	-DC_IN/ACN
PE2	P2	+DC_IN/ACL
PE3	LP1	CHASSIS

Table 3-1: 3U Input Power Elements

3.3.2. 6U POWER

Table 3-2 on page 12 defines the relationship between the power elements and power rails.

Power Element	J10 Pin #	Voltage
PE7	P7	-DC_IN/ACL/L1
PE6	P6	+DC_IN/L2
PE5	P5	-DC_IN/L3
PE4	P4	-DC_IN/ACN
N/C	P3	POS_FILT_OUT
N/C	P2	NEG_FILT_OUT
PE1	P1	CHASSIS

Table 3-2: AC Input Connector Pinout

The integrator is responsible for making certain that end users are not likely to make contact with any of the hazardous voltages.

3.4. ACCESSORY CONNECTIONS

3.4.1. DC OUTPUT RAILS

DC output rails from the PIB is done with M3 power elements.

The power elements are capable of supplying 60A when derated for a 30°C temperature rise. The backplane has been designed to allow the maximum power that the PSU power connectors are capable of supplying.

Table 3-3 on page 13 defines the relationship between the power elements, J10 and the corresponding output on the 3U PIB.

Power Element	J10 Pin #	Voltage
PE4	P6	PO1
PE5	LP2	PO2
PE6	P3	PO3
PE7/PE8	P4, P5	POWER_RETURN
PE18	A4, B4, C4, D4	3.3V_AUX
PE19	B3	+12V_AUX
PE20	C6	-12V_AUX

Table 3-3: 3U DC Output Power Elements

Table 3-4 on page 13 defines the relationship between the power elements, J11 and the corresponding output on the 6U PIB.

Power Element	J11 Pin #	Voltage
PE8	P10	PO1
PE9	P9	PO2
PE10/PE11	P5, P6	PO3
PE12-PE15	P1, P3, P4, P7, P8	POWER_RETURN
PE16	P2	3.3V_AUX
PE2	B3	+12V_AUX
PE3	C6	-12V_AUX

Table 3-4: 6U DC Output Power Elements

3.4.2. MISCELLANEOUS HEADERS

3.4.2.1. I/O Signals

The backplanes have a 26 pin shrouded header (P3) to accommodate all of the general purpose I/O from the PSUs. A compatible header is shown in Table 5-2 on page 25. Terminals will be series 090119. IDC headers are also available.

The system management signals are routed as differential pairs (100Ω) with SM0/SM1 forming one pair and SM2/SM3 forming the second pair.

The pairs have facilities for either single ended or differential termination via 0603 size resistors.

The PIB is shipped without any termination resistors installed.

Figure 3-2 on page 14 illustrates the possible resistor termination configurations. Note that only termination networks 1 and 3 are present on the PIBs. Termination networks 2 and 4 are assumed to be on a separate backplane.

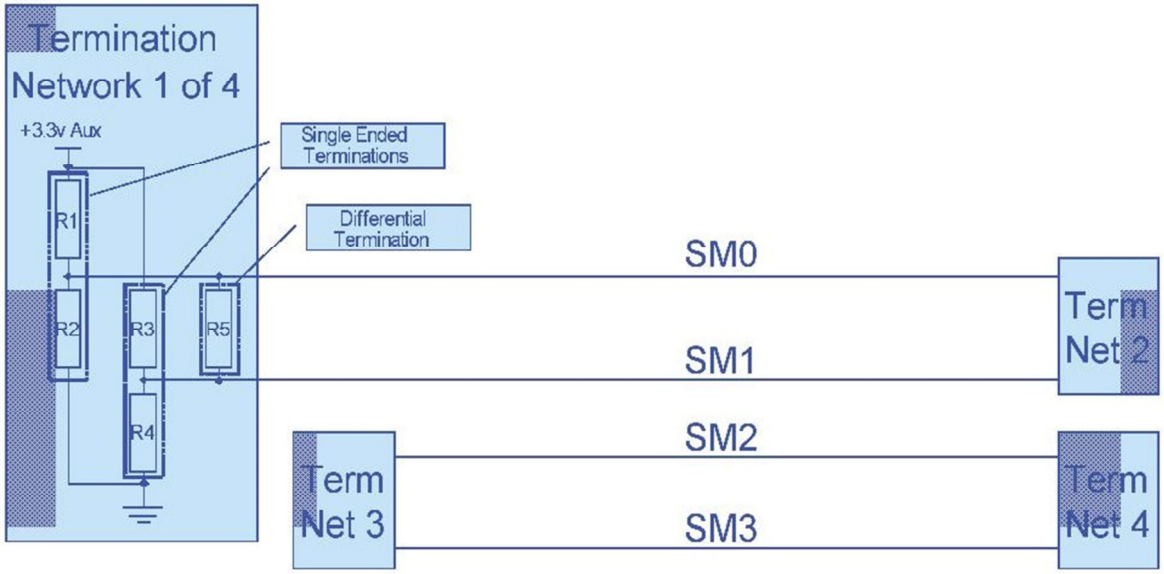


Figure 3-2: SM Bus Termination

Table 3-5 on page 14 provides the termination resistor mapping.

Resistor	R1	R2	R3	R4	R5
Network 1	R11	R12	R9	R10	R13
Network 3	R16	R17	R14	R15	R18

Table 3-5: SM Bus Termination Resistors

The SYSRESET* signal is terminated with a 220Ω resistor (R34) to 3.3V_AUX and a 1k8Ω resistor (R36) to SIGNAL_RETURN. A shunt (JP2) allows the termination to be enabled or disabled.

The VBAT signal has a shunt (JP1) to allow it to be connected to 3.3V_AUX.

The FAIL* signal is terminated with a 4k7Ω resistor (R35) to 3.3V_AUX. A shunt (JP3) allows the termination to be enabled or disabled.

The ENABLE* signal has a shunt (JP4) that allows it to be forced on.

There is a resistor (R1, 0603 package) that allows NED_RETURN to be connected to SIGNAL_RETURN.

Table 3-6 to Table 3-8 starting on page 15 define the pinout for the I/O connectors.

Signal	Pin #	Pin #	Signal
UD1	1	14	UD2
UD3	2	15	UD4
VBAT	3	16	FAIL*
INHIBIT*	4	17	ENABLE*
UD0	5	18	NED
SM0	6	19	NED_RETURN
SM1	7	20	SM2
SYSRESET*	8	21	SM3
PO1_SHARE	9	22	PO2_SHARE
PO3_SHARE	10	23	SIGNAL_RETURN
PO1_SEN_RTN	11	24	PO1_SENSE
PO2_SEN_RTN	12	25	PO2_SENSE
PO3_SEN_RTN	13	26	PO3_SENSE

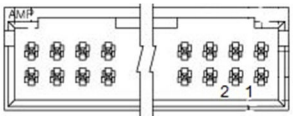


Table 3-6: 3U P3 I/O Connector

Signal	Pin #	Pin #	Signal
SM3	1	14	SM2
SM1	2	15	SM0
SIGNAL_RETURN	3	16	SIGNAL_RETURN
UD1	4	17	UD0
NED	5	18	NED_RETURN
UD2	6	19	VBAT
SIGNAL_RETURN	7	20	SIGNAL_RETURN
FAIL*	8	21	SYS_RESET*
INHIBIT*	9	22	ENABLE*
SIGNAL_RETURN	10	23	SIGNAL_RETURN
SIGNAL_RETURN	11	24	SIGNAL_RETURN
UD6	12	25	UD5
UD3	13	26	UD4

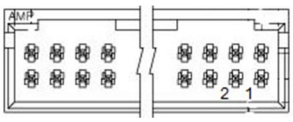


Table 3-7: 6U P3 I/O Connector

Signal	Pin #	Pin #	Signal
PO1_SEN_RTN	1	14	PO1_SENSE
PO2_SEN_RTN	2	15	PO2_SENSE
P03_SEN_RTN	3	16	PO3_SENSE
PO2_SHARE	4	17	P01_SHARE
SIGNAL_RETURN	5	18	PO3_SHARE

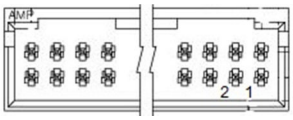


Table 3-8: 6U P7 I/O Connector

Refer to the PSU manufacturer's documentation for exact information on how to interface to the signals.

3.5. INSTALLING PLUG-IN MODULES IN YOUR BACKPLANE

The backplanes support either 3U or 6U VITA 62 compliant power supplies. For more information on module allocation, see the figures starting on page 9.

Do not use excessive force when installing or removing modules from the chassis. Use of excessive force can result in damage to the backplane and/or module.
Should excessive force be required, remove the module(s) and verify the alignment of the mechanicals and backplane.

There is no preset order to inserting modules into the backplane. Refer to the module and/or chassis User Manual(s) for more information on inserting modules.

SECTION FOUR

4. UNDERSTANDING YOUR BACKPLANE

These backplanes provide the system with the addition of one or more VITA 62 compliant power supply slots. Power from the backplanes is accomplished by either power elements alone or a combination of power elements and ¼" spade terminals.

4.1. BACKPLANE CONNECTORS

The complete list of connectors utilized on the backplanes is listed in Table 5-2 on page 25.

4.2. POWER CONNECTORS

The backplanes distribute DC power through the internal ½ and 1oz. copper planes which connect spade terminals and/or power elements.

The AC/DC input to the power supplies is provided by internal traces routed to support 40A of current carrying capability from the power elements.

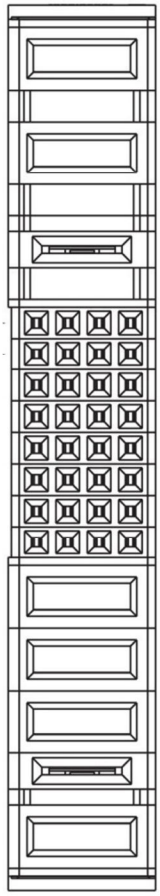
Multiple PIBs can be connected in load sharing mode.

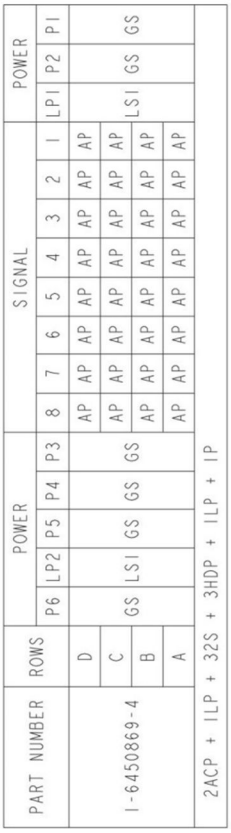
Remote voltage sensing for the power rails is employed by default.

4.2.1. 3U J10 CONNECTOR

Table 4-1 on page 18 displays the pinout for the 3U VITA 62 power supply connector.

Pin #	Current (A)	Signal
P1	40	-DC_IN/ACN
P2	40	+DC_IN/ACL
LP1	20	CHASSIS
A1	<1	UD1
B1	<1	UD2
C1	<1	UD3
D1	<1	UD4
S2	<1	VBAT
B2	<1	FAIL*
C2	<1	INHIBIT*
D2	<1	ENABLE*
A3	<1	UD0
B3	<1.5	+12V_AUX
C3	<1	NED
D3	<1	NED_RETURN
A4	<1.5	3.3V_AUX
B4	<1.5	3.3V_AUX
C4	<1.5	3.3V_AUX
D4	<1.5	3.3V_AUX
A5	<1	GA0*
B5	<1	GA1*
C5	<1	SM0
D5	<1	SM1
A6	<1	SM2
B6	<1	SM3
C6	<1.5	-12V_AUX
D6	<1	SYSRESET*
A7	<1	PO1_SHARE
B7	<1	PO2_SHARE
C7	<1	PO3_SHARE
D7	<1	SIGNAL_RETURN
A8	<1	PO1_SENSE
B8	<1	PO2_SENSE
C8	<1	PO3_SENSE
D8	<1	SENSE_RETURN
P3	40	PO3
P4	40	POWER_RETURN
P5	40	POWER_RETURN
LP2	20	PO2
P6	40	PO1





The mechanical location of the power supply connectors is designed to meet the VITA 62 specification.

Table 4-1: 3U J10 Connector Pinout and Outline

4.2.2. 6U J10/J11 CONNECTORS

Table 4-2 on page 19 displays the pinout for the 6U J10 VITA 62 power supply connector.

Table 4-3 on page 20 displays the pinout for the 6U J11 VITA 62 power supply connector.

Pin #	Current (A)	Signal
P7	40	-DC_IN/ACL/L1
P6	40	+DC_IN/L2
P5	40	-DC_IN/L3
P4	40	-DC_IN/ACN
P3	40	POS_FILT_OUT
P2	40	NEG_FILT_OUT
P1	40	CHASSIS

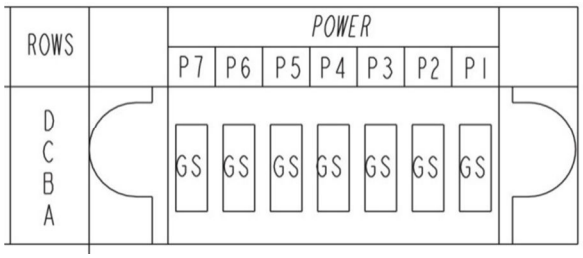
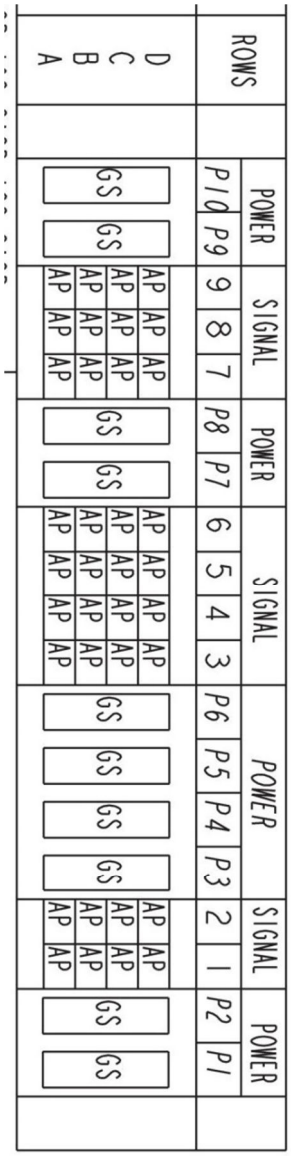


Table 4-2: 6U J10 Connector Pinout and Outline

Pin #	Current (A)	Signal
P10	40	P01
P9	40	P02
A9	<1	PO1_SENSE
B9	<1	PO2_SENSE
C9	<1	PO3_SENSE
D9	<1	UD0
A8	<1	PO1_SENSE_RTN
B8	<1	PO2_SENSE_RTN
C8	<1	PO3_SENSE_RTN
D8	<1	UD1
A7	<1	PO1_SHARE
B7	<1	PO2_SHARE
C7	<1	PO3_SHARE
D7	<1	SIGNAL_RETURN
P8	40	POWER_RETURN
P7	40	POWER_RETURN
A6	<1	SM2
B6	<1	SM3
C6	<1.5	-12V_AUX
D6	<1	SYSRESET*
A5	<1	GAP*
B5	<1	GA4*
C5	<1	SM0
D5	<1	SM1
A4	<1	GA3*
B4	<1	GA2*
C4	<1	GA1*
D4	<1	GA0*
A3	<1	UD2
B3	<1.5	+12V_AUX
C3	<1	NED
D3	<1	NED_RETURN
P6	40	PO3
P5	40	P03
P4	40	POWER_RETURN
P3	40	POWER_RETURN
A2	<1	VBAT
B2	<1	FAIL*
C2	<1	INHIBIT*
D2	<1	ENABLE*



Pin #	Current (A)	Signal
A1	<1	UD3
B1	<1	UD4
C1	<1	UD5
D1	<1	UD6
P2	40	3.3V_AUX
P1	40	POWER_RETURN

Table 4-3: 6U J11 Connector Pinout and Outline

The mechanical location of the power supply connectors is designed to meet the VITA 62 specification.

4.3. GEOGRAPHIC ADDRESSING

4.3.1. 3U

There is a 4 pin header (P1) for setting the geographic address of the power supply slot at J10 and one (P2) for the slot at J20.

Pin 1 is denoted by the white triangle

Table 4-4 on page 20 displays how the address can be set for each of the PSU slots.

P1, P2		
Addr	Pin 3,4 (GA1)	Pins 1,2 (GA0)
0	Shorted	Shorted
1	Shorted	Open
2	Open	Shorted
3	Open	Open

Table 4-4: 3U Geographic Addressing

4.3.2. 6U

Geographic addressing on the 6U is accomplished by the use of 0603 resistor sites.

Table 4-5 on page 21 provides the list of resistor combinations for addresses 1 to 21.

Address	R24 (GAP*)	R23 (GA4*)	R22 (GA3*)	R21 (GA2*)	R20 (GA1*)	R19 (GA0*)
1						Installed
2					Installed	
3	Installed				Installed	Installed
4				Installed		
5	Installed			Installed		Installed
6	Installed			Installed	Installed	
7				Installed	Installed	Installed
8			Installed			
9	Installed		Installed			Installed
10	Installed		Installed		Installed	

Address	R24 (GAP*)	R23 (GA4*)	R22 (GA3*)	R21 (GA2*)	R20 (GA1*)	R19 (GA0*)
11			Installed		Installed	Installed
12	Installed		Installed	Installed		
13			Installed	Installed		Installed
14			Installed	Installed	Installed	
15	Installed		Installed	Installed	Installed	Installed
16		Installed				
17	Installed	Installed				Installed
18	Installed	Installed			Installed	
19		Installed			Installed	Installed
20	Installed	Installed		Installed		
21		Installed		Installed		Installed

Table 4-5: 6U Geographic Addressing Resistors

Solder bridges can be utilized in lieu of resistors.

PSU addresses must not be duplicated if they are on the same management bus.

4.4. SLOT KEYING

4.4.1. 3U KEYING

The upper and lower keying features allow for 5 possible key positions.

Table 4-6 and Table 4-7 starting on page 21, display the valid key positions.

Key Position	Voltage Range
0°	18V to 36V
45°	0V to 18V
90°	36V to 85V
270°	85V to 265V
315°	265V to 500V

Table 4-6: 3U Key 1 Positions

WARNING: Although the keying allows for voltages greater than 240V, the connector is not capable of passing UL testing beyond 240V.

Key Position	Input AC vs. DC	Intended Use Of Output	Nominal Output Voltage for Each Output Pin		
			PO1	PO2	PO3
0°	DC Input	Final Power Out	12 VDC (VS1)	3.3 VDC (VS2)	5 VDC (VS3)
45°	AC Input		12 VDC (VS1)	3.3 VDC (VS2)	5 VDC (VS3)
90°	If nominal input < 85V then input is DC. If nominal input ≥ 85V then input is AC	Intermediate Power Out	18 to 36 VDC	Return for PO1	N/C
270°			36 to 72 VDC	Return for PO1	N/C
315°			200 to 400 VDC	Return for PO1	N/C

Table 4-7: 3U Key 2 Positions

The alignment keys are connected to chassis ground and are each capable of carrying 20 Amps to the chassis ground attachment points.

4.4.2. 6U KEYING

The upper and lower keying features allow for 5 possible key positions.

Table 4-8, Table 4-9 and Table 4-10 starting on page 22, display the valid key positions.

Key Position	Voltage Range
0°	18V to 36V
45°	0V to 18V
90°	36V to 85V
270°	85V to 265V
315°	265V to 500V

Table 4-8: 6U Key 1 Positions

WARNING: Although the keying allows for voltages greater than 240V, the connector is not capable of passing UL testing beyond 240V.

Key Position	DC vs. AC & Number of Phases
0°	DC
45°	Single phase AC
90°	Three phase AC
270°	Reserved
315°	Reserved

Table 4-9: 6U Key 2 Positions

Key Position	Intended Use Of Output	Nominal Output Voltage for Each Output Pin		
		PO1	PO2	PO3
0°	Final Power with both 12V & 5V	12 VDC (VS1, VS2)	12 VDC (VS1, VS2)	5 VDC (VS3)
45°	Final Power with more 12V & no 5V	12 VDC (VS1, VS2)	12 VDC (VS1, VS2)	12 VDC (VS1, VS2) or N/C
90°	Intermediate Power	18 to 36 VDC	18 to 36 VDC	18 to 36 VDC or N/C
270°	Final with both 48V & 5V or Intermediate Power	36 to 72 VDC (VS1 for 48 DC)	Return for PO1 (VS2 for 48 VDC)	N/C
315°	Intermediate Power	200 to 400 VDC	Return for PO1	N/C

Table 4-10: 6U Key 3 Positions

The alignment keys are connected to chassis ground and are each capable of carrying 20 Amps to the chassis ground attachment points.

4.5. VOLTAGE SENSING

By default, the backplanes are configured for remote voltage sensing.

On the 3U, this is done via connector P3. On the 6U, this is done via connector P7.

To enable local voltage sensing, solder bridges need to be added for each rail.

On PO1, this is done by bridging SS1 (PO1_SENSE) and SS4 (PO1_SEN_RTN). On PO2 by bridging (SS2 PO2_SENSE) and SS5 (PO2_SEN_RTN). And on PO5 by bridging SS3 (PO3_SENSE) and SS6 (PO3_SEN_RTN).

WARNING: Only configure for one type of voltage sensing.

4.6. REGULATORY AND SAFETY

The backplanes have been designed to comply with the following standards:

- EN 69050
- UL 1950

A clearance of 2.5mm has been provided between AC voltages and chassis ground on all external layers. A clearance of 5mm has been provided between AC and secondary voltages on all internal layers. A clearance of 0.4mm has been provided between primary and secondary voltages on all internal layers.

SECTION FIVE

5. APPENDIX A

5.1. ACRONYMS

The following list provides definitions of acronyms used throughout this document.

ACRONYM	DEFINITION
AdvancedTCA®	Advanced Telecom Computing Architecture
BP	Backplane
CompactPCI®	Compact Peripheral Component Interconnect
CPSB	Compact Packet Switching Backplane
ECN	Engineering Change Notice
FCC	Federal Communications Commission
GA	Geographical Addressing
GPIO	General Purpose Input Output
HP	Horizontal Pitch (aperture width)
I/O	Input/Output
I^2C	Intelligent Interface Controller
N/C	Not Connected
P/N	Part Number
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PICMG®	PCI Industrial Computer Manufacturers Group
SBC	Single Board Computer
SMB	System Management Bus
SMD	System Management Device
U	Unit (vertical height)
UL	Underwriter's Laboratory
V(I/O)	Voltage (Input/Output)

5.2. TORQUE VALUES

Table 5-1 on page 24 displays the recommended torque values for fasteners used on the backplanes.

Screws	Torque
M2.5	0.68 Nm (6 lbf.in)
M3	1.14 Nm (10 lbf.in)

Table 5-1: Recommended Torque Values

List of Connectors

Table 5-2 on page 25 displays the list of connectors utilized on the backplanes.

Description	Reference	Vendor	Conn. P/N	Rating	Mating Conn. P/N
3U					
Power	J10, J20	TE	1-6450869-4	94V-0	6450849-7
6U					
Power	J10, J20	TE	6450863-5	94V-0	6450843-6
Power & I/O	J11, J21	TE	1-6450869-0	94V-0	6450849-6
2x5 Header	P7	TE	5-102699-4	94V-0	87631-6 *
2x6 Header	P1, P2	Samtec	TSW-106-08-F-D	94V-0	Shunt (0.1”)
Common					
Power (M3)	PE01-PE20	Wurth	7461057	94V-0	
		ERNI	225681	94V-0	
1x2 Header	JP1-JP4	Samtec	TSW-102-08-G-S	94V-0	Shunt (0.1”)
2x13 Header	P3	TE	6-102699-2	94V-0	2-87631-2 *
Key	K[1-3]01	TE	1-1469491-2	94V-0	

Table 5-2: Backplane Connectors

* Crimps for shrouded headers are 6-87523-9 for 24-20 Ga wire.

Document Part Number: UM 01A000102-A01.docx

Issue Date: 10-May-2018

Executive Member

Pixus Technologies Inc. • 50 Bathurst Drive, Unit 6, Waterloo, Ontario Canada N2V 2C5 • (519) 885-5775 •
www.pixustechnologies.com

Printed in Canada