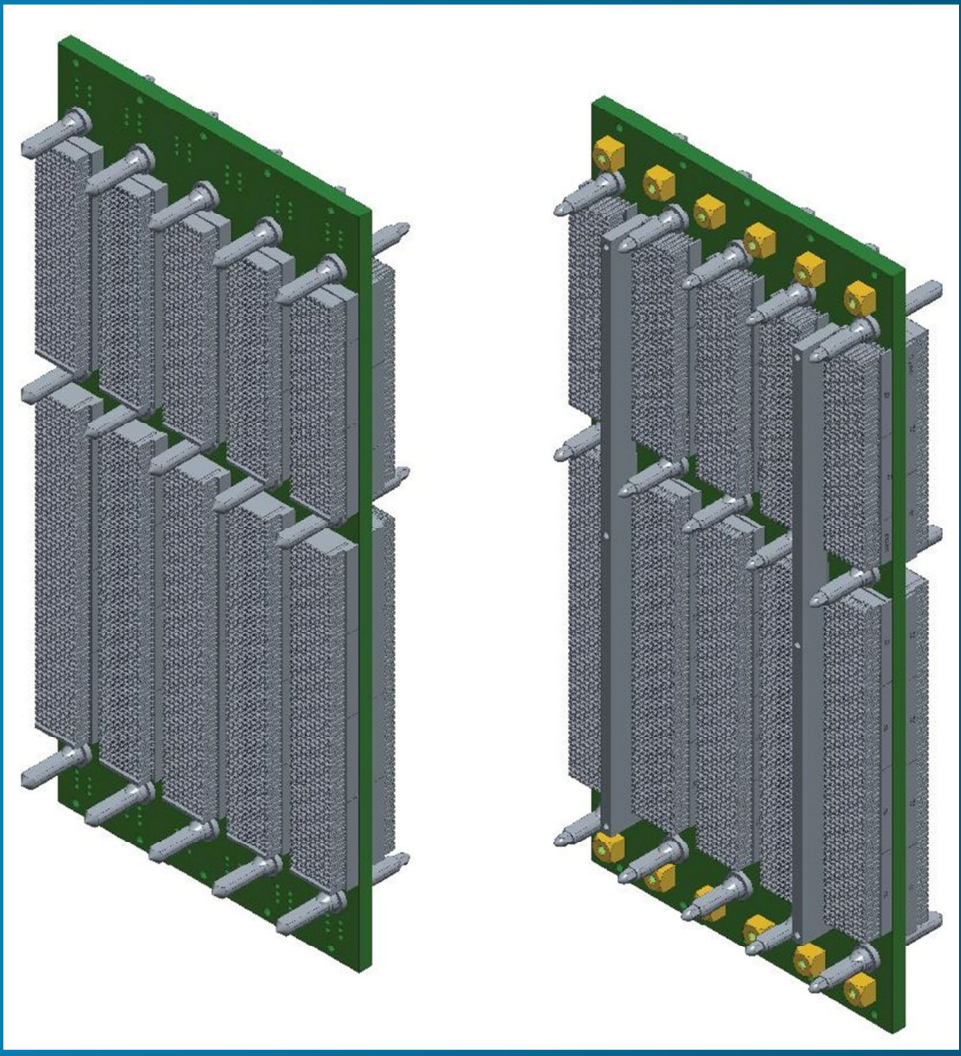
USER GUIDE



5 SLOT OPENVPX BACKPLANE
BKP6-CEN05-11.2.5-3+

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Issue	Date	Description
1.0	19-Oct-2018	Product release

TYPOGRAPHICAL CONVENTIONS USED IN THIS DOCUMENT

Items	Convention
You will see the following icons periodically throughout this manual:	
	The **WARNING** icon cautions you against an action or treatment that could threaten the responsiveness of the equipment or the integrity of your current work.
	The **INSPECT** icon alerts the reader to follow inspection instructions to ensure product is not damaged and in operational order.
	The **NOTE** icon notifies you of the information that makes a procedure easier or clarifies an earlier description.
Headings, titles, sections or words of importance.	These items appear in **bold** typeface. Example: **Any changes or modifications…….**
Variable placeholders, references to other documents, new or special terminology, and emphasis.	These items appear in *italic* typeface. Example: *Table 3-1*, displays……
References to chapters and sections of documents, and citations of messages displayed to users.	These items appear in “quotation marks.” Example: For more information, refer to “Connections”, section 3….

Revision History

Revision	Date	Description	Author
1.0	19-Oct-2018	Released for product approvals	

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SECTION ONE

1. INTRODUCTION

This section provides a brief overview about Pixus Technologies Inc. This section describes the following:

- 1.1 Pixus Technologies Inc.
- 1.2 Contact Information
- 1.3 Background Information
- 1.4 Applicability

1.1. PIXUS TECHNOLOGIES INC.

Pixus Technologies specializes in the design and manufacture of electronic packaging solutions for the global embedded computer market. The company is comprised of three business units: backplanes, Enclosure & System Solutions and Components.

Leveraging over 20 years of innovative product development, Pixus Technologies' embedded backplanes and systems are focused primarily on xTCA, OpenVPX, CompactPCI, PCIe and custom designs. The company offers unsurpassed thermal management solutions, creative design innovations, and backplane design expertise. Pixus also offers modular 19" rackmount enclosure solutions and instrument cases to a wide range of industries, as well as precision components such as front panels, handles, and card guides.

The approach to each customer requirement is a simple consultative philosophy - understand the specific program requirements and create the best solution that meets the time frame, architecture, technology and cost objectives.

1.2. CONTACT INFORMATION

For questions about the Pixus product or about Pixus in general, please contact us using the following information:

Phone Number: (519) 885-5775
Fax Number: (226) 444-0225
Web Address: www.pixustechnologies.com
Mailing Address: Pixus Technologies Inc.
50 Bathurst Drive, Unit 6
Waterloo, Ontario
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For Pixus product support, see the Pixus web site: www.pixustechnologies.com

1.3. BACKGROUND INFORMATION

When designing OpenVPX® systems, use the following documents for reference:

- ANSI/VITA® 62.0 Modular Power Supply Standard
- ANSI/VITA® 48.0 Mechanical Specification for Microcomputers Using Ruggedized Enhanced Design Implementation (REDI)
- ANSI/VITA® 48.1 Mechanical Specification for Microcomputers Using REDI Air Cooling
- ANSI/VITA® 46.0-2007 VPX Baseline Standard
- ANSI/VITA® 46.1-2007 VMEbus Signal Mapping on VPX
- ANSI/VITA® 46.3-2012 Serial RapidIO® on VPX Fabric Connector
- ANSI/VITA® 46.4-2012 PCI Express® on VPX Fabric Connector
- ANSI/VITA® 46.6-2013 Gigabit Ethernet Control Plane on VPX
- ANSI/VITA® 46.7-2012 Ethernet on VPX Fabric Connector
- ANSI/VITA® 46.8-VDSTU Infiniband® on the VPX Fabric Connector
- ANSI/VITA® 46.9-2010 PMC/XMC Rear I/I Signal Mapping on 3U and 6U VPX Module
- ANSI/VITA® 46.10-2009 Rear Transition Module for VPX
- ANSI/VITA® 46.11-VDSTU System Management for VPX
- ANSI/VITA® 46.9 PMC/XMC Rear I/O Fabric Signal Mapping on 3U and 6U VPX Modules Standard
- ANSI/VITA® 65.0-2017 OpenVPX® System Standard
- ANSI/VITA® 65.1-2017 OpenVPX® System Standard – Profile Tables
- ANSI/VITA® 68.0-VDSTU VPX Compliance Channel
- ANSI/VITA® 68.1-VDSTU VPX Compliance Channel – Fixed Signal Integrity Budget
- RoHS 2011/65/EU

1.4. APPLICABILITY

This User Guide is applicable to the following model(s):

Model	Description
VPX60-05-XX-CC11A31-0	5 Slot OpenVPX Backplane BKP6-CEN05-11.2.5-3+

Table 1-1: Applicability

SECTION TWO

2. FEATURES

The backplane has been designed with the following features:

- Conformance to VITA 65.x BKP6-CEN05-11.2.5-3+ profile.
- Support for 5 6U 5HP Modules.
- 10Gbps minimum signaling rate.
- ANSI/VITA® 65.0 and 65.1 compliant.
- Mechanical conformance to 153.16mm L x 128.7mm W x 5.4mm H.
- Sixteen layer construction.
- Power elements for primary power input.
- Individual 5-pin headers for JTAG connectivity at each slot.
- Two 8-pin headers for access to the system management bus and control signals.
- Support for 5 rear I/O Modules.
- Switch slot will conform to VITA 65.1 SLT6-SWH-16U20F-10.4.2 profile.
- Payload slots will conform to VITA 65.1 SLT6-PAY-4F1Q2U2T-10.2.1 profile.
- Stiffeners for added strength.

Figure 2-1 illustrates the major features of the backplane, showing approximate locations for all connectors. Objects drawn as solid lines are on the front side of the backplane.

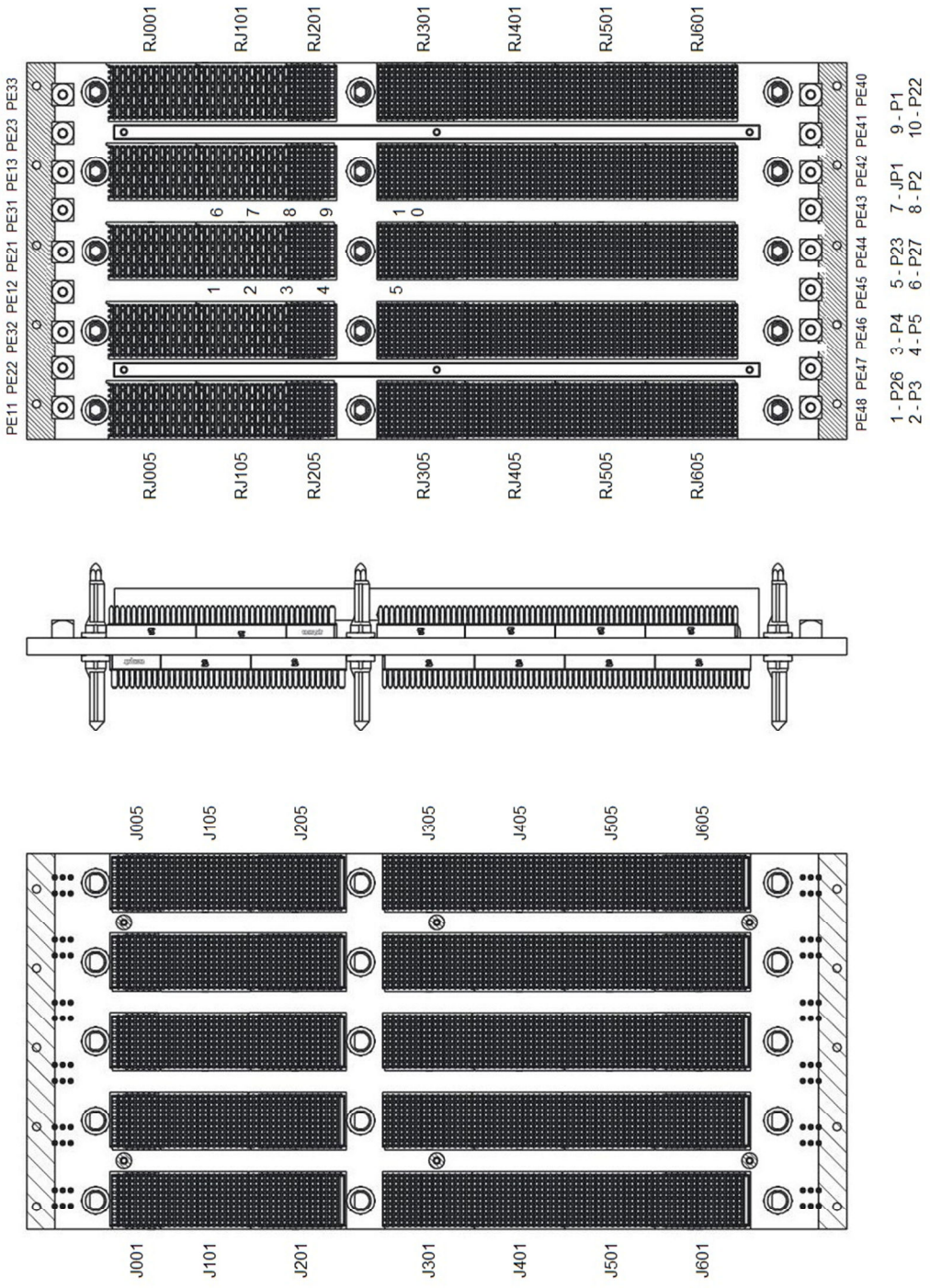

Figure 2-1: Connector Locations

SECTION THREE

3. QUICK START

The backplane complies with the VITA standards as they were when the backplane was created.

This chapter will provide an overview of basic operating procedures, including the following:

- Inspecting Your Backplane
- Installing Your Backplane In A Subrack
- Accessory Connections

3.1. INSPECTING YOUR BACKPLANE

Take great care when handling the backplane. Improper handling could cause damage to the connector pins.
Always handle the backplane from the edges, never the connectors.

The first item that must be done before starting to utilize your backplane is to perform a thorough inspection.

During the course of handling, shipping and assembly, pins, mounting screws and other items could become damaged and/or loose. Operating a damaged backplane could cause serious damage to the backplane and/or devices that interface to it.

Take a few minutes to visually inspect that all of the connector pins are straight, screws are tight, etc.

Repair any bent pins, loose screws, etc. before proceeding. If damage to the backplane is deemed too extensive, call Pixus Customer Service for assistance on how to proceed.

3.2. INSTALLING YOUR BACKPLANE IN A SUBRACK

The backplane mounts into a sub-rack using M2.5 screws along the rows of mounting holes situated at the top and bottom end of each slot, with all mounting holes connecting to chassis ground with the possible exception of one.

The mounting rail areas of the backplane have exposed strips of copper that are connected directly to the chassis ground of the backplane.

The backplane must be mounted in the sub-rack with insulator strips between it and the rails. Applications where conductive strips are utilized must be inspected to make sure there is no electrical contact between the rails and any device on the backplane.

As stated above, there is possibly one mounting screw that allows digital ground to be tied to chassis (frame) ground. The mounting hole that connects to digital ground is marked with the corresponding symbol (⏚) on the bottom silkscreen.

The arrow in Figure 3-1 illustrates the screw location for the single ground tie point.

Refer to the subrack user guide for information on torque limits for the mounting screws.

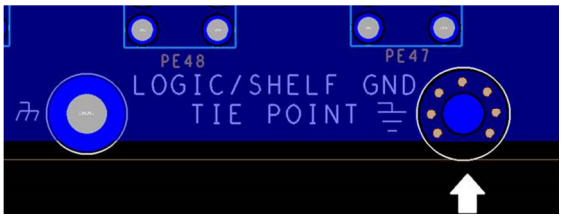

Figure 3-1: Digital Ground – Chassis Ground Tie Point

3.3. ACCESSORY CONNECTIONS

3.3.1. MISCELLANEOUS HEADERS

3.3.1.1. JTAG

Each slot has a 5 pin header (P1-5]) to allow access to the slot's JTAG signals.

Refer to Table 5-2 for a suitable mating connector and wire crimps.

Table 3-1 displays the pinout for the JTAG headers along with the corresponding pin on the slot

Pin #	Signal	Backplane Pin
1	TRST_[1:5]	J0[01:5] a7
2	TMS_[1:5]	J0[01:5] b7
3	TDI_[1:5]	J0[01:5] e7
4	TDO_[1:5]	J0[01:5] f7
5	TCK_[1:5]	J0[01:5] i7

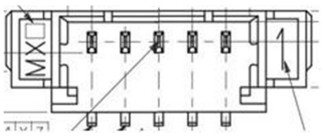

Table 3-1: JTAG Connectors

3.3.1.2. VBAT

One 3-pin header (P26) is supplied on the rear side for external connection to VBAT and 3.3V_AUX.

A standard 0.100" shunt is provided to connect VBAT to either GND or 3.3V_AUX. By default, the connection is to 3.3V_AUX.

Refer to Table 5-2 for a suitable mating connector and wire crimps for other applications.

Table 3-2 illustrates the pinout for the VBAT connector.

Pin #	Signal
1	GND
2	VBAT
3	3.3V_AUX

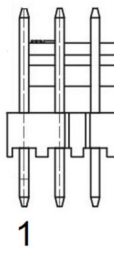

Table 3-2: VBAT Connector Pinout

3.3.1.3. System Management

There are two 8 pin headers (P22, P23) to allow access to the System Management signals.

Refer to Table 5-2 for a suitable mating connector and wire crimps.

Table 3-3 on page 12 displays the pinout for the System Management headers.

Pin #	Signal (P22)	Signal (P23)
8	SM1	SM3
7	SM0	SM2
6	SYSRESET*	SYSRESET*
5	GND	GND
4	NVMRO	NVMRO
3	MSK_RST*	MSK_RST*
2	GND	GND
1	3.3V_AUX	3.3V_AUX

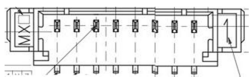

Table 3-3: System Management Connectors

Note that MSK_RST* is only present on these pins when it is bussed to all slots.

3.3.1.4. NVMRO

The backplane busses this signal to all slots.

Jumper JP1 allow for the signal to be grounded on the backplane.

3.4. INSTALLING PLUG-IN MODULES IN YOUR BACKPLANE

The backplane supports up to 5 OpenVPX® Plug-In Modules.

Refer to section 4.3 for information on which Plug-In Module goes into which slot.

The latching/unlatching mechanism on the Plug-In Module should suffice for insertion/extraction.

Do not use excessive force when installing or removing Plug-In Modules from the chassis. Use of excessive force can result in damage to the backplane and/or Plug-In Module. Should excessive force be required, remove the Plug-In Module(s) and verify the alignment of the mechanicals and backplane.

There is no preset order to inserting Plug-In Modules into the backplane. Refer to the Plug-In Module and/or chassis User Manual(s) for more information on inserting Plug-In Modules.

SECTION FOUR

4. UNDERSTANDING YOUR BACKPLANE

4.1. BACKPLANE CONNECTORS

The complete list of connectors utilized on the backplane is listed in Table 5-2.

4.2. POWER CONNECTORS

Slots are powered through power elements and for lower slot count backplanes, a combination of power elements and a header. The backplane distributes DC power (12V, 5V, 3.3V, 3.3V_AUX, +12V_AUX & -12V_AUX) to each slot through the internal copper planes.

The power elements are capable of providing 60 Amps in a 70° C ambient environment.

The AUX power connector (P27) for the narrower backplanes is rated at 4 Amps per pin. There is no derating information available.

4.2.1. VS1, VS2, VS3 AND GND

Per the specification, each slot can source 22A on Vs1, Vs2 and Vs3.

The Vs1, Vs2 and Vs3 power elements (as applicable) are on the top rear of the backplane.

Vs1 power elements are referenced from PE11-PE17 and are bused on the backplane.

Vs2 power elements are referenced from PE21-PE27 and are bused on the backplane.

Vs3 power elements are referenced from PE31-PE37 and are bused on the backplane.

There is one corresponding GND power element for each Vs[1-3] power element. GND power elements are on the lower rear of the backplane.

Ground power elements are referenced from PE40-PE60 and are bussed on the backplane.

4.2.2. AUX POWER

Per the specification, each slot can source 1A on 3.3V_AUX, +12V_AUX and -12V_AUX.

Where space permits, this is done with power elements. If present, these will be located on the top rear of the backplane.

Where space does not permit, it is done with a PCB-wire header (P27).

Refer to Table 5-2 for a suitable mating connector and wire crimps. Table 4-1 provides the pinout for the AUX power connections.

Pin #	Signal	Signal
1	+12V_AUX	PE71
2	+12V_AUX	
3	3.3V_AUX	PE72
4	3.3V_AUX	
5	-12V_AUX	PE73
6	-12V_AUX	

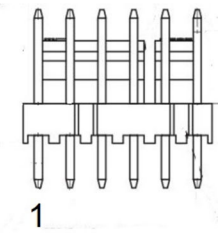

Table 4-1: AUX Power Connections

4.2.3. SAFETY GROUND

The top and bottom mounting rail surfaces are the connection point to safety ground.

The alignment keys each have a minimum 20 A path to the connection point.

Some backplanes will have a feature for allowing safety ground to be tied to logic ground. Refer to section 3.2.

4.2.4. DECOUPLING

Each slot has provisions for decoupling capacitors.

A high frequency decoupling capacitor (0.1 uf) is provided for each power rail at each slot.

Provisions for optional bulk filtering capacitors are provided for each power rail at each slot. These can be requested as an option when noisy power rails are expected.

4.3. SLOT IDENTIFICATION

4.3.1. SLOT KEYING

3U backplanes have 2 alignment/keying devices as required in the ANSI/VITA 46.0 specification.

6U backplanes have 3 alignment/keying devices as required in the ANSI/VITA 46.0 specification.

Table 4-2 provides the as-shipped keying settings for 3U and 6U backplanes.

Slot#	3U		6U		
	Key 1	Key 2	Key 1	Key 2	Key 3
1	270°	270°	315°	270°	270°
2	315°	270°	315°	315°	270°
3	0°	270°	315°	0°	270°
4	45°	270°	315°	45°	270°
5	90°	270°	315°	90°	270°
6	270°	315°	315°	270°	315°
7	315°	315°	315°	315°	315°
8	0°	315°	315°	0°	315°
9	45°	315°	315°	45°	315°
10	90°	315°	315°	90°	315°

Slot#	3U		6U		
	Key 1	Key 2	Key 1	Key 2	Key 3
11	270°	0°	315°	270°	0°
12	315°	0°	315°	315°	0°
13	0°	0°	315°	0°	0°
14	45°	0°	315°	45°	0°
15	90°	0°	315°	90°	0°
16	270°	45°	315°	270°	45°
17	315°	45°	315°	315°	45°
18	0°	45°	315°	0°	45°
19	45°	45°	315°	45°	45°
20	90°	45°	315°	90°	45°
21	270°	90°	315°	270°	90°

Table 4-2 Slot Keying

4.3.2. SLOT NUMBERING

Slots are be numbered according to the ANSI/VITA 46 specification.

The leftmost slot (viewed from the front) always has a geographic address of 1 and will increment by one.

Table 4-3 illustrates the slot geographic address on the various length backplanes.

Slot#	GAP*	GA4*	GA3*	GA2*	GA1*	GA0*
1	Open	Open	Open	Open	Open	GND
2	Open	Open	Open	Open	GND	Open
3	GND	Open	Open	Open	GND	GND
4	Open	Open	Open	GND	Open	Open
5	GND	Open	Open	GND	Open	GND
6	GND	Open	Open	GND	GND	Open
7	Open	Open	Open	GND	GND	GND
8	Open	Open	GND	Open	Open	Open
9	GND	Open	GND	Open	Open	GND
10	GND	Open	GND	Open	GND	Open
11	Open	Open	GND	Open	GND	GND
12	GND	Open	GND	GND	Open	Open
13	Open	Open	GND	GND	Open	GND
14	Open	Open	GND	GND	GND	Open
15	GND	Open	GND	GND	GND	GND
16	Open	GND	Open	Open	Open	Open
17	GND	GND	Open	Open	Open	GND
18	GND	GND	Open	Open	GND	Open

Slot#	GAP*	GA4*	GA3*	GA2*	GA1*	GA0*
19	Open	GND	Open	Open	GND	GND
20	GND	GND	Open	GND	Open	Open
21	Open	GND	Open	GND	Open	GND

Table 4-3 Geographic Addressing

4.4. BACKPLANE TOPOLOGY

Figure 4-1 illustrates the backplane topology. The dotted lines from the Payload and Switch slots are signals that are available to the complementary RTM.

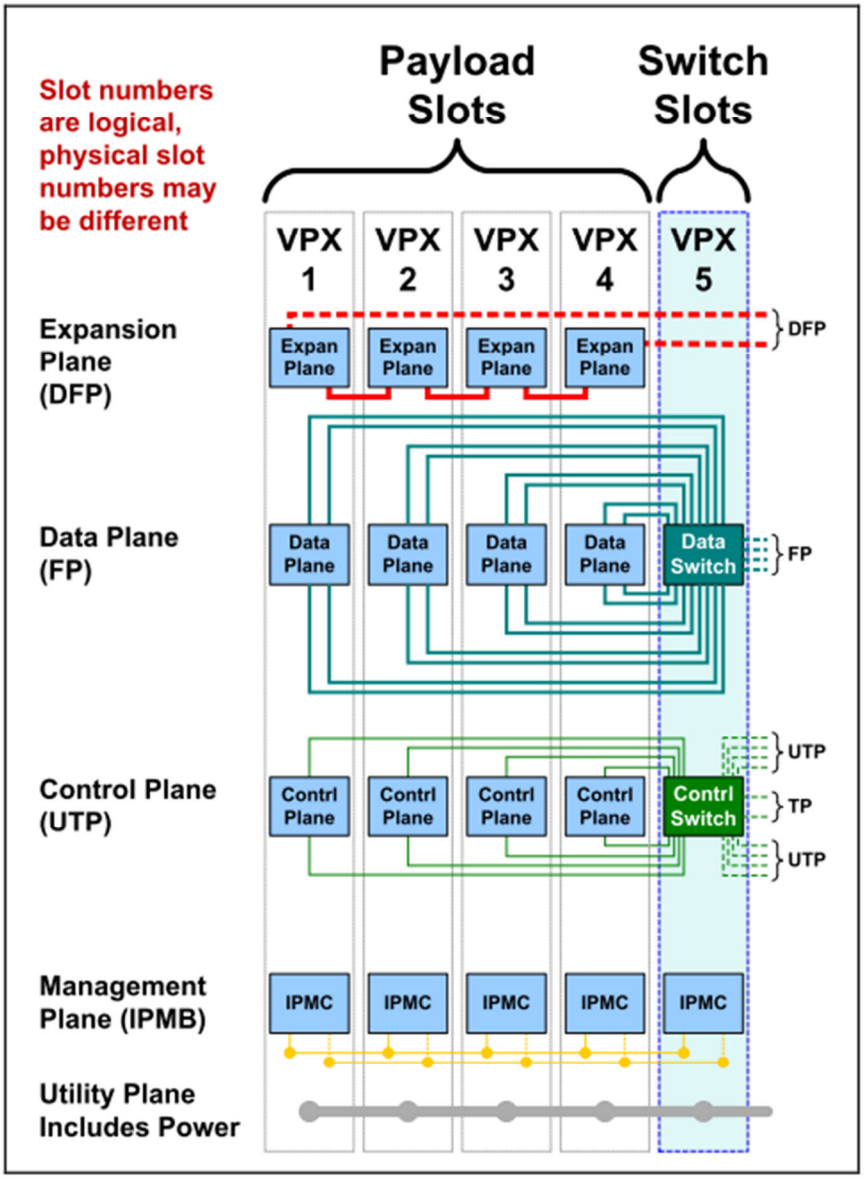

Figure 4-1: Backplane Topology

4.5. BACKPLANE PROFILE COMPATIBILITY

Table 4-4 displays the list of Backplane Profiles that the backplane is compatible with.

Slot profile information is also provided.

A “+” at the end of the profile name indicates that this particular profile was not approved as part of ANSI/VITA 65.1 at the time of publication of this document.

Backplane Profile Names	Mechanical		Channel Gbaud Rate					Payload		Control and Data Plane Switch	
	Pitch (in)	RTM conn	Control Plane (UTP)	Data Plane (FP)	Expansion Plane (DFP)			Slot(s)	Slot Profile	Slot(s)	Slot Profile
BKP6-CEN05-11.2.5-1	1.0	46.10	10	10	10			1-4	SLT6-PAY-4F1Q2U2T-10.2.1	5	SLT6-SWH-16U20F-10.4.2

Table 4-4: Backplane Profile Compatibility

4.6. SYS_CON*

This signal is pulled low on physical slot 1.

Each slot has the option of having this signal pulled low.

Consult Pixus Technologies for information on how this can be accomplished.

4.7. CONTROL PLANE

The backplane has the Control Plane Ports connected as shown in Table 4-5.

Logical Payload Slot	Payload Control Plane Port	Switch Control Plane Port
1	CPutp01	CPutp01
1	Cputp02	CPutp05
2	CPutp01	CPutp02
2	Cputp02	CPutp06
3	CPutp01	CPutp03
3	Cputp02	CPutp07
4	CPutp01	CPutp04
4	Cputp02	CPutp08

Table 4-5 Control Plane Port Allocation

4.8. EXPANSION PLANE

The backplane has the Control Plane Ports connected as shown in Figure 4-2.

Dotted lines are signals that are available to the adjacent RTM.

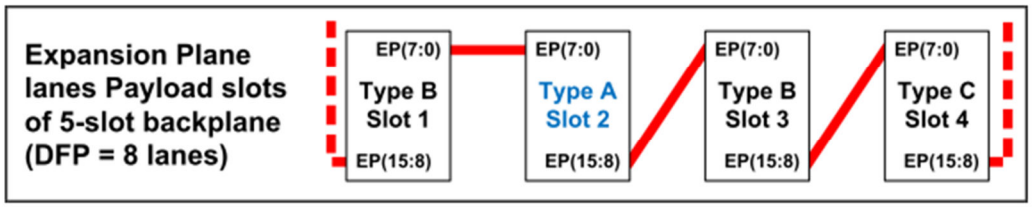

Figure 4-2: Expansion Plane Interconnect

4.9. DATA PLANE

The backplane has the Data Plane Ports connected as shown in Table 4-6.

Dotted lines are signals that are available to the adjacent RTM.

Slot/Channel	DP01	DP02	DP03	DP04
1	VPX05-DP01	VPX05-DP05	VPX05-DP09	VPX05-DP13
2	VPX05-DP02	VPX05-DP06	VPX05-DP10	VPX05-DP14
3	VPX05-DP03	VPX05-DP07	VPX05-DP11	VPX05-DP15

Slot/Channel	DP01	DP02	DP03	DP04
4	VPX05-DP04	VPX05-DP08	VPX05-DP12	VPX05-DP16

Table 4-6 Data Plane Port Allocation

4.10. CONNECTOR PINOUTS

4.10.1. J0

Table 4-7 defines the signals present on J0 for all slots.

	Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Vs1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2	Vs2
2	Vs1	Vs1	Vs1	Vs1	No Pad*	Vs2	Vs2	Vs2	Vs2
3	Vs3	Vs3	Vs3	Vs3	No Pad*	Vs3	Vs3	Vs3	Vs3
4	GND	SM2	SM3	GND	-12V_Aux	GND	SYSRESET*	NVMRO	GND
5	GND	GAP*	GA4*	GND	3.3V_Aux	GND	SM0	SM1	GND
6	GND	GA3*	GA2*	GND	+12V_Aux	GND	GA1*	GA0*	GND
7	TCK	GND	GND	TDO	TDI	GND	GND	TMS	TRST*
8	GND	REF_CLK-	REF_CLK+	GND	GND	AUX_CLK-	AUX_CLK+	GND	GND

Table 4-7 J0 Pin Assignment

4.10.1.1. REF/AUX_CLK

This are bussed differential pairs with an impedance of 130 Ohms +-10%, terminated with 61.9 Ohm +-1% resistors.

4.10.1.2. System Management

These signals are bused to all slots with facilities for single-ended and differential termination at both ends of the signals.

When configured for IPMB operation, each signal must be pulled high to 3.3V_AUX by a 2k49 Ohm +-1% resistor at one end only.

Figure 4-3 illustrates the termination resistor configuration for the System Management bus.

Table 4-8 provides the mapping for the SM Bus termination resistor pairs (Term1/Term2 and Term3/Term4). Note that the resistor sites are all 0603 sized.

Signal	R1	R2	R3	R4	R5
SM0	R4/R11	R5/R12			R6/R13
SM1			R2/R9	R3/R10	R6/R13
SM2	R21/R16	R22/R17			R23/R18
SM3			R19/R14	R20/R15	R23/R18

Table 4-8 SM Bus Termination Resistor Mapping

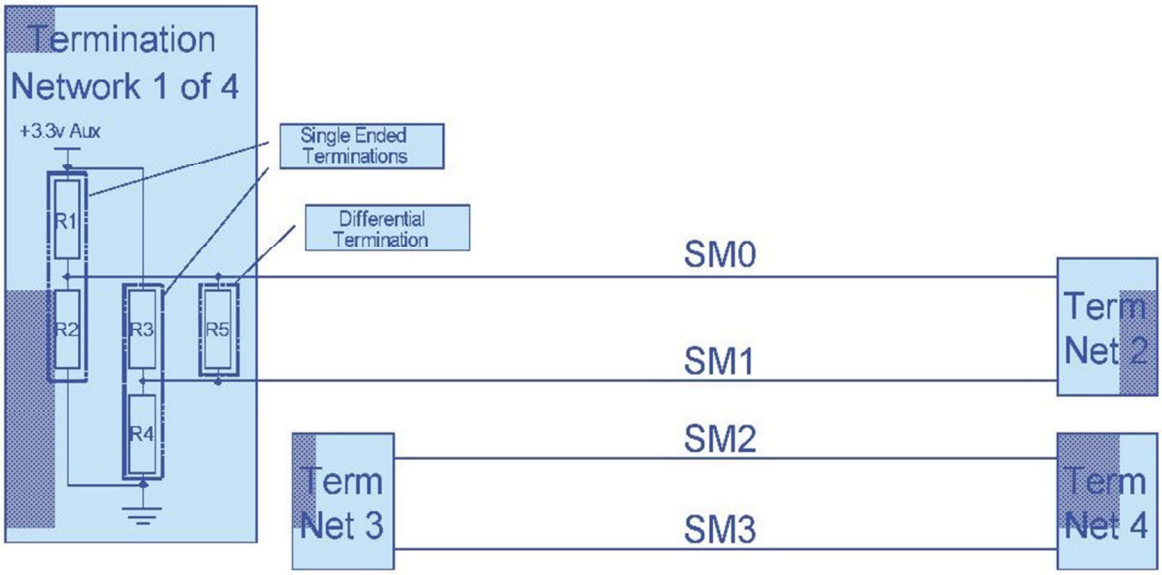

Figure 4-3 SM Bus Terminations

4.10.1.3. NVMRO

This signal is bussed to all slots.

Jumper JP1 allows for the signal to be grounded on the backplane.

4.10.1.4. SYSRESET*

This signal is bussed to all slots and is pulled high to 3.3V_AUX by a 220 Ohm +-5% resistor and pulled low by a 1k8 Ohm +-5% resistor.

4.10.2. PAYLOAD SLOT PINOUT

Table 4-9, Table 4-10 and Table 4-11 provide the pin assignments for J1, J2 and J4 on the Payload slots.

4.10.3. GDISCRETE1

The backplane busses this signal to all slots.

The single-ended impedance is 50 Ohms.

470 Ohm +-5% resistors terminate the signal at both end of the backplane to 3.3V_AUX.

4.10.4. SYS_CON*

Slot number 1 (leftmost) has this pin connected to ground.

To allow for ambiguity in the specification, all slots have provision for connecting this pin to ground.

4.10.5. UD

These pins are application specific and not defined. They could be bussed or individually routed to a connection point.

4.10.6. MASKABLERESET*

This pin is application specific and not defined. It could be bussed or individually routed to a connection point. This backplane busses the signal and routes it to P22 and P23.

4.10.7. P1-VBAT

The backplane busses this signal to all slots and to P26. Refer to Section 3.3.1.2.

Plug-In Module P1		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Port 1	GDiscrete1	GND	GND-J1	DP01-T0-	DP01-T0+	GND	GND-J1	DP01-R0-	DP01-R0+
2		GND	DP01-T1-	DP01-T1+	GND-J1	GND	DP01-R1-	DP01-R1+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	DP01-T2-	DP01-T2+	GND	GND-J1	DP01-R2-	DP01-R2+
4		GND	DP01-T3-	DP01-T3+	GND-J1	GND	DP01-R3-	DP01-R3+	GND-J1	GND
5	Data Plane Port 2	SYS_CON*	GND	GND-J1	DP02-T0-	DP02-T0+	GND	GND-J1	DP02-R0-	DP02-R0+
6		GND	DP02-T1-	DP02-T1+	GND-J1	GND	DP02-R1-	DP02-R1+	GND-J1	GND
7		Reserved	GND	GND-J1	DP02-T2-	DP02-T2+	GND	GND-J1	DP02-R2-	DP02-R2+
8		GND	DP02-T3-	DP02-T3+	GND-J1	GND	DP02-R3-	DP02-R3+	GND-J1	GND
9	Data Plane Port 3	UD	GND	GND-J1	DP03-T0-	DP03-T0+	GND	GND-J1	DP03-R0-	DP03-R0+
10		GND	DP03-T1-	DP03-T1+	GND-J1	GND	DP03-R1-	DP03-R1+	GND-J1	GND
11		UD	GND	GND-J1	DP03-T2-	DP03-T2+	GND	GND-J1	DP03-R2-	DP03-R2+
12		GND	DP03-T3-	DP03-T3+	GND-J1	GND	DP03-R3-	DP03-R3+	GND-J1	GND
13	Data Plane Port 4	UD	GND	GND-J1	DP04-T0-	DP04-T0+	GND	GND-J1	DP04-R0-	DP04-R0+
14		GND	DP04-T1-	DP04-T1+	GND-J1	GND	DP04-R1-	DP04-R1+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	DP04-T2-	DP04-T2+	GND	GND-J1	DP04-R2-	DP04-R2+
16		GND	DP04-T3-	DP04-T3+	GND-J1	GND	DP04-R3-	DP04-R3+	GND-J1	GND

Table 4-9 Payload J1 Pin Assignment

Plug-In Module P2				Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Backplane J2				Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	X16 using [15:0]	x8 using [7:0]	x4 using [3:0]	UD	GND	GND-J2	EP00-T-	EP00-T+	GND	GND-J2	EP00-R-	EP00-R+
2				GND	EP01-T-	EP01-T+	GND-J2	GND	EP01-R-	EP01-R+	GND-J2	GND
3				UD	GND	GND-J2	EP02-T-	EP02-T+	GND	GND-J2	EP02-R-	EP02-R+
4				GND	EP03-T-	EP03-T+	GND-J2	GND	EP03-R-	EP03-R+	GND-J2	GND
5			x4 using [7:4]	UD	GND	GND-J2	EP04-T-	EP04-T+	GND	GND-J2	EP04-R-	EP04-R+
6				GND	EP05-T-	EP05-T+	GND-J2	GND	EP05-R-	EP05-R+	GND-J2	GND
7				UD	GND	GND-J2	EP06-T-	EP06-T+	GND	GND-J2	EP06-R-	EP06-R+
8				GND	EP07-T-	EP07-T+	GND-J2	GND	EP07-R-	EP07-R+	GND-J2	GND
9		x8 using[15:8]	x4 using [11:8]	UD	GND	GND-J2	EP08-T-	EP08-T+	GND	GND-J2	EP08-R-	EP08-R+
10				GND	EP09-T-	EP09-T+	GND-J2	GND	EP09-R-	EP09-R+	GND-J2	GND
11				UD	GND	GND-J2	EP10-T-	EP10-T+	GND	GND-J2	EP10-R-	EP10-R+
12				GND	EP11-T-	EP11-T+	GND-J2	GND	EP11-R-	EP11-R+	GND-J2	GND
13			x4 using[15:12]	UD	GND	GND-J2	EP12-T-	EP12-T+	GND	GND-J2	EP12-R-	EP12-R+
14				GND	EP13-T-	EP13-T+	GND-J2	GND	EP13-R-	EP13-R+	GND-J2	GND
15				UD	GND	GND-J2	EP14-T-	EP14-T+	GND	GND-J2	EP14-R-	EP14-R+
16				GND	EP15-T-	EP15-T+	GND-J2	GND	EP15-R-	EP15-R+	GND-J2	GND

Table 4-10 Payload J2 Pin Assignment

Plug-In Mod P4		Row G	Row F	Row E Even	Row E Odd	Row D	Row C	Row B Even	Row B Odd	Row A
Bplane J4		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	User Defined	UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
2		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
3		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
4		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
5		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
6		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
7		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
8		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
9		UD	GND	GND-J4	UD	UD	GND	GND-J4	UD	UD
10		GND	UD	UD	GND-J4	GND	UD	UD	GND-J4	GND
11	2 UTP	UD	GND	GND-J4	CPutp02-T-	CPutp02-T+	GND	GND-J4	CPutp02-R-	CPutp02-R+
12		GND	CPutp01-T-	CPutp01-T+	GND-J4	GND	CPutp01-R-	CPutp01-R+	GND-J4	GND
13	Control Plane 2 TPs	UD	GND	GND-J4	CPtp02-DB-	CPtp02-DB+	GND	GND-J4	CPtp02-DA-	CPtp02-DA+
14		GND	CPtp02-DD-	CPtp02-DD+	GND-J4	GND	CPtp02-DC-	CPtp02-DC+	GND-J4	GND
15		UD	GND	GND-J4	CPtp01-DB-	CPtp01-DB+	GND	GND-J4	CPtp01-DA-	CPtp01-DA+
16		GND	CPtp01-DD-	CPtp01-DD+	GND-J4	GND	CPtp01-DC-	CPtp01-DC+	GND-J4	GND

Table 4-11 Payload J4 Pin Assignment

Table 4-12 to Table 4-17 provide the pin assignments for J1 to J6 on the Switch slot.

Plug-In Module P1		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J1		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	CPlane Inter-SW UTPs Ports 1 – 4	GDiscrete1	GND	GND-J1	CSutp01-T-	CSutp01-T+	GND	GND-J1	CSutp01-R-	CSutp01-R+
2		GND	CSutp02-T-	CSutp02-T+	GND-J1	GND	CSutp02-R-	CSutp02-R+	GND-J1	GND
3		P1-VBAT	GND	GND-J1	CSutp03-T-	CSutp03-T+	GND	GND-J1	CSutp03-R-	CSutp03-R+
4		GND	CSutp04-T-	CSutp04-T+	GND-J1	GND	CSutp04-R-	CSutp04-R+	GND-J1	GND
5	Control Plane Payload UTPs Ports 1 – 12	SYS_CON*	GND	GND-J1	CPutp01-T-	CPutp01-T+	GND	GND-J1	CPutp01-R-	CPutp01-R+
6		GND	CPutp02-T-	CPutp02-T+	GND-J1	GND	CPutp02-R-	CPutp02-R+	GND-J1	GND
7		Reserved	GND	GND-J1	CPutp03-T-	CPutp03-T+	GND	GND-J1	CPutp03-R-	CPutp03-R+
8		GND	CPutp04-T-	CPutp04-T+	GND-J1	GND	CPutp04-R-	CPutp04-R+	GND-J1	GND
9		UD	GND	GND-J1	CPutp05-T-	CPutp05-T+	GND	GND-J1	CPutp05-R-	CPutp05-R+
10		GND	CPutp06-T-	CPutp06-T+	GND-J1	GND	CPutp06-R-	CPutp06-R+	GND-J1	GND
11		UD	GND	GND-J1	CPutp07-T-	CPutp07-T+	GND	GND-J1	CPutp07-R-	CPutp07-R+
12		GND	CPutp08-T-	CPutp08-T+	GND-J1	GND	CPutp08-R-	CPutp08-R+	GND-J1	GND
13		UD	GND	GND-J1	CPutp09-T-	CPutp09-T+	GND	GND-J1	CPutp09-R-	CPutp09-R+
14		GND	CPutp10-T-	CPutp10-T+	GND-J1	GND	CPutp10-R-	CPutp10-R+	GND-J1	GND
15		Maskable Reset*	GND	GND-J1	CPutp11-T-	CPutp11-T+	GND	GND-J1	CPutp11-R-	CPutp11-R+
16		GND	CPutp12-T-	CPutp12-T+	GND-J1	GND	CPutp12-R-	CPutp12-R+	GND-J1	GND

Table 4-12 Switch J1 Pin Assignment

Plug-In Module P2		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J2		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane FP Port 16	UD	GND	GND-J2	DP16-T0-	DP16-T0+	GND	GND-J2	DP16-R0-	DP16-R0+
2		GND	DP16-T1-	DP16-T1+	GND-J2	GND	DP16-R1-	DP16-R1+	GND-J2	GND
3		UD	GND	GND-J2	DP16-T2-	DP16-T2+	GND	GND-J2	DP16-R2-	DP16-R2+
4		GND	DP16-T3-	DP16-T3+	GND-J2	GND	DP16-R3-	DP16-R3+	GND-J2	GND
5	Data Plane FP Port 15	UD	GND	GND-J2	DP15-T0-	DP15-T0+	GND	GND-J2	DP15-R0-	DP15-R0+
6		GND	DP15-T1-	DP15-T1+	GND-J2	GND	DP15-R1-	DP15-R1+	GND-J2	GND
7		UD	GND	GND-J2	DP15-T2-	DP15-T2+	GND	GND-J2	DP15-R2-	DP15-R2+
8		GND	DP15-T3-	DP15-T3+	GND-J2	GND	DP15-R3-	DP15-R3+	GND-J2	GND
9	Data Plane FP Port 14	UD	GND	GND-J2	DP14-T0-	DP14-T0+	GND	GND-J2	DP14-R0-	DP14-R0+
10		GND	DP14-T1-	DP14-T1+	GND-J2	GND	DP14-R1-	DP14-R1+	GND-J2	GND
11		UD	GND	GND-J2	DP14-T2-	DP14-T2+	GND	GND-J2	DP14-R2-	DP14-R2+
12		GND	DP14-T3-	DP14-T3+	GND-J2	GND	DP14-R3-	DP14-R3+	GND-J2	GND
13	Data Plane FP Port 13	UD	GND	GND-J2	DP13-T0-	DP13-T0+	GND	GND-J2	DP13-R0-	DP13-R0+
14		GND	DP13-T1-	DP13-T1+	GND-J2	GND	DP13-R1-	DP13-R1+	GND-J2	GND
15		UD	GND	GND-J2	DP13-T2-	DP13-T2+	GND	GND-J2	DP13-R2-	DP13-R2+
16		GND	DP13-T3-	DP13-T3+	GND-J2	GND	DP13-R3-	DP13-R3+	GND-J2	GND

Table 4-13 Switch J2 Pin Assignment

Plug-In Module P3		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J3		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Payload FP Port 12	UD	GND	GND-J3	DP12-T0-	DP12-T0+	GND	GND-J3	DP12-R0-	DP12-R0+
2		GND	DP12-T1-	DP12-T1+	GND-J3	GND	DP12-R1-	DP12-R1+	GND-J3	GND
3		UD	GND	GND-J3	DP12-T2-	DP12-T2+	GND	GND-J3	DP12-R2-	DP12-R2+
4		GND	DP12-T3-	DP12-T3+	GND-J3	GND	DP12-R3-	DP12-R3+	GND-J3	GND
5	Data Plane Payload FP Port 11	UD	GND	GND-J3	DP11-T0-	DP11-T0+	GND	GND-J3	DP11-R0-	DP11-R0+
6		GND	DP11-T1-	DP11-T1+	GND-J3	GND	DP11-R1-	DP11-R1+	GND-J3	GND
7		UD	GND	GND-J3	DP11-T2-	DP11-T2+	GND	GND-J3	DP11-R2-	DP11-R2+
8		GND	DP11-T3-	DP11-T3+	GND-J3	GND	DP11-R3-	DP11-R3+	GND-J3	GND
9	Data Plane Payload FP Port 10	UD	GND	GND-J3	DP10-T0-	DP10-T0+	GND	GND-J3	DP10-R0-	DP10-R0+
10		GND	DP10-T1-	DP10-T1+	GND-J3	GND	DP10-R1-	DP10-R1+	GND-J3	GND
11		UD	GND	GND-J3	DP10-T2-	DP10-T2+	GND	GND-J3	DP10-R2-	DP10-R2+
12		GND	DP10-T3-	DP10-T3+	GND-J3	GND	DP10-R3-	DP10-R3+	GND-J3	GND
13	Data Plane Payload FP Port 9	UD	GND	GND-J3	DP09-T0-	DP09-T0+	GND	GND-J3	DP09-R0-	DP09-R0+
14		GND	DP09-T1-	DP09-T1+	GND-J3	GND	DP09-R1-	DP09-R1+	GND-J3	GND
15		UD	GND	GND-J3	DP09-T2-	DP09-T2+	GND	GND-J3	DP09-R2-	DP09-R2+
16		GND	DP09-T3-	DP09-T3+	GND-J3	GND	DP09-R3-	DP09-R3+	GND-J3	GND

Table 4-14 Switch J3 Pin Assignment

Plug-in Module P4		Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J4		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Payload FP Port 8	UD	GND	GND-J4	DP08-T0-	DP08-T0+	GND	GND-J4	DP08-R0-	DP08-R0+
2		GND	DP08-T1-	DP08-T1+	GND-J4	GND	DP08-R1-	DP08-R1+	GND-J4	GND
3		UD	GND	GND-J4	DP08-T2-	DP08-T2+	GND	GND-J4	DP08-R2-	DP08-R2+
4		GND	DP08-T3-	DP08-T3+	GND-J4	GND	DP08-R3-	DP08-R3+	GND-J4	GND
5	Data Plane Payload FP Port 7	UD	GND	GND-J4	DP07-T0-	DP07-T0+	GND	GND-J4	DP07-R0-	DP07-R0+
6		GND	DP07-T1-	DP07-T1+	GND-J4	GND	DP07-R1-	DP07-R1+	GND-J4	GND
7		UD	GND	GND-J4	DP07-T2-	DP07-T2+	GND	GND-J4	DP07-R2-	DP07-R2+
8		GND	DP07-T3-	DP07-T3+	GND-J4	GND	DP07-R3-	DP07-R3+	GND-J4	GND
9	Data Plane Payload FP Port 6	UD	GND	GND-J4	DP06-T0-	DP06-T0+	GND	GND-J4	DP06-R0-	DP06-R0+
10		GND	DP06-T1-	DP06-T1+	GND-J4	GND	DP06-R1-	DP06-R1+	GND-J4	GND
11		UD	GND	GND-J4	DP06-T2-	DP06-T2+	GND	GND-J4	DP06-R2-	DP06-R2+
12		GND	DP06-T3-	DP06-T3+	GND-J4	GND	DP06-R3-	DP06-R3+	GND-J4	GND
13	Data Plane Payload FP Port 5	UD	GND	GND-J4	DP05-T0-	DP05-T0+	GND	GND-J4	DP05-R0-	DP05-R0+
14		GND	DP05-T1-	DP05-T1+	GND-J4	GND	DP05-R1-	DP05-R1+	GND-J4	GND
15		UD	GND	GND-J4	DP05-T2-	DP05-T2+	GND	GND-J4	DP05-R2-	DP05-R2+
16		GND	DP05-T3-	DP05-T3+	GND-J4	GND	DP05-R3-	DP05-R3+	GND-J4	GND

Table 4-15 Switch J4 Pin Assignment

Plug-In Module P5		Row G	Row F	Row E		Row D	Row C	Row B		Row A
Bplane J5		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Pay-load FP Port 4	UD	GND	GND-J5	DP04-T0-	DP04-T0+	GND	GND-J5	DP04-R0-	DP04-R0+
2		GND	DP04-T1-	DP04-T1+	GND-J5	GND	DP04-R1-	DP04-R1+	GND-J5	GND
3		UD	GND	GND-J5	DP04-T2-	DP04-T2+	GND	GND-J5	DP04-R2-	DP04-R2+
4		GND	DP04-T3-	DP04-T3+	GND-J5	GND	DP04-R3-	DP04-R3+	GND-J5	GND
5	Data Plane Pay-load FP Port 3	UD	GND	GND-J5	DP03-T0-	DP03-T0+	GND	GND-J5	DP03-R0-	DP03-R0+
6		GND	DP03-T1-	DP03-T1+	GND-J5	GND	DP03-R1-	DP03-R1+	GND-J5	GND
7		UD	GND	GND-J5	DP03-T2-	DP03-T2+	GND	GND-J5	DP03-R2-	DP03-R2+
8		GND	DP03-T3-	DP03-T3+	GND-J5	GND	DP03-R3-	DP03-R3+	GND-J5	GND
9	Data Plane Pay-load FP Port 2	UD	GND	GND-J5	DP02-T0-	DP02-T0+	GND	GND-J5	DP02-R0-	DP02-R0+
10		GND	DP02-T1-	DP02-T1+	GND-J5	GND	DP02-R1-	DP02-R1+	GND-J5	GND
11		UD	GND	GND-J5	DP02-T2-	DP02-T2+	GND	GND-J5	DP02-R2-	DP02-R2+
12		GND	DP02-T3-	DP02-T3+	GND-J5	GND	DP02-R3-	DP02-R3+	GND-J5	GND
13	Data Plane Pay-load FP Port 1	UD	GND	GND-J5	DP01-T0-	DP01-T0+	GND	GND-J5	DP01-R0-	DP01-R0+
14		GND	DP01-T1-	DP01-T1+	GND-J5	GND	DP01-R1-	DP01-R1+	GND-J5	GND
15		UD	GND	GND-J5	DP01-T2-	DP01-T2+	GND	GND-J5	DP01-R2-	DP01-R2+
16		GND	DP01-T3-	DP01-T3+	GND-J5	GND	DP01-R3-	DP01-R3+	GND-J5	GND

Table 4-16 Switch J5 Pin Assignment

Plug-In Module P6		Row G	Row F	Row E		Row D	Row C	Row B		Row A
				Even	Odd			Even	Odd	
Bplane J6		Row i	Row h	Row g	Row f	Row e	Row d	Row c	Row b	Row a
1	Data Plane Inter-SW FP Port 4	UD	GND	GND-J6	DS04-T0-	DS04-T0+	GND	GND-J6	DS04-R0-	DS04-R0+
2		GND	DS04-T1-	DS04-T1+	GND-J6	GND	DS04-R1-	DS04-R1+	GND-J6	GND
3		UD	GND	GND-J6	DS04-T2-	DS04-T2+	GND	GND-J6	DS04-R2-	DS04-R2+
4		GND	DS04-T3-	DS04-T3+	GND-J6	GND	DS04-R3-	DS04-R3+	GND-J6	GND
5	Data Plane Inter-SW FP Port 3	UD	GND	GND-J6	DS03-T0-	DS03-T0+	GND	GND-J6	DS03-R0-	DS03-R0+
6		GND	DS03-T1-	DS03-T1+	GND-J6	GND	DS03-R1-	DS03-R1+	GND-J6	GND
7		UD	GND	GND-J6	DS03-T2-	DS03-T2+	GND	GND-J6	DS03-R2-	DS03-R2+
8		GND	DS03-T3-	DS03-T3+	GND-J6	GND	DS03-R3-	DS03-R3+	GND-J6	GND
9	Data Plane Inter-SW FP Port 2	UD	GND	GND-J6	DS02-T0-	DS02-T0+	GND	GND-J6	DS02-R0-	DS02-R0+
10		GND	DS02-T1-	DS02-T1+	GND-J6	GND	DS02-R1-	DS02-R1+	GND-J6	GND
11		UD	GND	GND-J6	DS02-T2-	DS02-T2+	GND	GND-J6	DS02-R2-	DS02-R2+
12		GND	DS02-T3-	DS02-T3+	GND-J6	GND	DS02-R3-	DS02-R3+	GND-J6	GND
13	Data Plane Inter-SW FP Port 1	UD	GND	GND-J6	DS01-T0-	DS01-T0+	GND	GND-J6	DS01-R0-	DS01-R0+
14		GND	DS01-T1-	DS01-T1+	GND-J6	GND	DS01-R1-	DS01-R1+	GND-J6	GND
15		UD	GND	GND-J6	DS01-T2-	DS01-T2+	GND	GND-J6	DS01-R2-	DS01-R2+
16		GND	DS01-T3-	DS01-T3+	GND-J6	GND	DS01-R3-	DS01-R3+	GND-J6	GND

Table 4-17 Switch J6 Pin Assignment

4.11. REGULATORY AND SAFETY

The backplanes have been designed to comply with the following standards:

- EN 69050
- UL 1950

A clearance of 2.5 mm has been provided between AC voltages and chassis ground on all external layers. A clearance of 5 mm has been provided between AC and secondary voltages on all internal layers. A clearance of 0.4 mm has been provided between primary and secondary voltages on all internal layers.

SECTION FIVE

5. APPENDIX A

5.1. ACRONYMS

The following list provides definitions of acronyms used throughout this document.

ACRONYM	DEFINITION
AdvancedTCA®	Advanced Telecom Computing Architecture
BP	Backplane
CompactPCI®	Compact Peripheral Component Interconnect
CPSB	Compact Packet Switching Backplane
ECN	Engineering Change Notice
FCC	Federal Communications Commission
GA	Geographical Addressing
GPIO	General Purpose Input Output
HP	Horizontal Pitch (aperture width)
I/O	Input/Output
I^2C	Intelligent Interface Controller
N/C	Not Connected
P/N	Part Number
PCB	Printed Circuit Board
PCI	Peripheral Component Interconnect
PICMG®	PCI Industrial Computer Manufacturers Group
SBC	Single Board Computer
SMB	System Management Bus
SMD	System Management Device
U	Unit (vertical height)
UL	Underwriter's Laboratory
V(I/O)	Voltage (Input/Output)

5.2. TORQUE VALUES

Table 5-1 displays the recommended torque values for fasteners used on the backplanes.

Screws	Torque
Power Element (M3)	0.5 Nm (4.43 lbf.in)
Keyed Guide Pin	0.45 Nm (4 in-lb)

Table 5-1: Recommended Torque Values

5.3. LIST OF CONNECTORS

Table 5-2 displays the list of connectors utilized on the backplane.

Description	Reference	Vendor	Conn. P/N	Rating	Mating Conn. P/N
Power Elements	PE11-PE13 PE21-PE23 PE31-PE33 PE40-PE48	ERNI/ Wurth	225693/7461057	94V-0	
Management 1x8	P22, P23	Molex	53398-0871	94V-0	51021-0800
JTAG Connector	P1-P5	Molex	53398-0571	94V-0	51021-0500
MultiGig Keyed Guide Pin 24mm 3.6-7.5mm	K1[01-05] K2[01-05] K3[01-05]	TE	1410956-1	94V-0	
MultiGig RT T2.8" Half Left	J001-J005 RJ201, RJ204	TE/ept	1410186-2 / 308-52200-42	94V-0	
MultiGig RT T2.8" Full Center	J101-J105 J301-J305 J401-J405 J501-J505 RJ105 RJ401-RJ404 RJ501-RJ504 RJ601-RJ605	TE/ept	1410140-2 / 308-50100-42	94V-0	
MultiGig RT T2.8" Full Center Rear w 1-8	RJ001-RJ004	TE/ept	1410965-2 / 308-50102-42	94V-0	
MultiGig RT T2.8" Full Right	J201-J205 J601-J605 RJ301- RJ304	TE/ept	1410142-2 / 308-51100-42	94V-0	
MultiGig RT T2.8" Full Center Rear w/o 1-8	RJ005	TE/ept	1410964-2 / 308-50101-42	94V-0	
Aux Power (1x6)	P27	Molex	22-11-2066	94V-0	22012061
VBat (1x3)	P26	Molex	22-11-2036	94V-0	22012031
NVMRO	JP1	Samtec	TSW-102-08-G-S	94V-0	Shunt

Crimps for P26, P27 - 8550102

Crimps for P1 – P5 – 500588100

Table 5-2: Backplane Connectors

The mating headers for P26 and P27 may not have a 1-to-1 pin alignment.

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