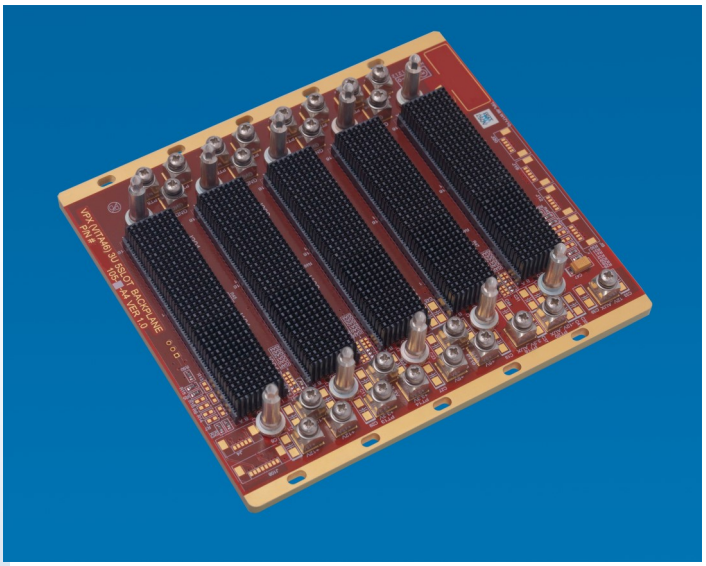
OpenVPX Backplanes—3U

VPX30 Backplanes



VPX30 KEY FEATURES

- Compliant to latest VITA 65 specifications
- Various OpenVPX profiles—contact Pixus for details
- 2, 3, 5, 6, 8, 9, 12, and 18 slots standard (contact Pixus for other sizes as all may not be listed)
- Typically 1.0” pitch, but some sizes (18-slot, etc in 0.8” pitch)
- 3U backplane design
- Data rate options up to 40Gbps and beyond
- Selectable rear IO options
- Fast turnaround, superior performance
- Customization available
- Conformal coating optional

OpenVPX is a process that defines system level VPX interoperability for multi-vendor, multi-module, integrated systems environment. The OpenVPX process defines clear interoperability points necessary for integration between Module to Module, Module to Backplane and Chassis.

Pixus has an experience team of OpenVPX experts and can help you find or create the OpenVPX backplane profile for your application. We offer various data signal speed options and have optional testing services. Pixus is IS09001:2015 and ITAR registered.

The backplanes are typically 1.0” pitch, but 0.8” pitch is available in some configurations. Contact Pixus for details.

Pixus Technologies can modify this product to meet special customer requirements without NRE (minimum order placement is required).

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Specifications

Architecture		
Physical	Dimensions	Height: 3U
		Width: Depending on slot #
		Pitch: 1.0" or 0.8" standard
	Connectors	MultiGig RT-2
	Layers	14-18 layers typical
Standards		
VITA	Type	VITA 65 for OpenVPX
	Type	VITA 46 for VPX base specification
Configuration		
Power		3.3V, 3.3V AUX, 5V, 12V options
Environmental	Temperature	Operating temperature: -40° to +85°C
		Storage temperature: -55° to +90°C
	PCB	FR406 or equivalent, Nelco4000-13SI or equivalent for higher speeds
		(consult Pixus)
	PCB traces	2 oz. power and ground standard
Conformal coating		Upon request (See page 6 selection "J" for available options)
Other		
MTBF	MIL Handbook 217-F @ TBD Hrs.	
Certifications	Designed to meet FCC, CE and EN/UL/TUV certifications where applicable	
Warranty	Two years	
Trademarks and logos	The Pixus Logo is a registered trademark of Pixus Technologies Inc. other registered trademarks are the property of their respective owners. Specs. subject to change without notice.	

Connectors & Signals

Connector Ratings

Multi-Gig RT-2:

Operating Voltage: 50 Volts AC peak or DC
Current: 1 Ampere at <30°C (single circuit, free air)
Temperature: -55 to 105°C
Low level contact resistance, circuit: 80 milliohms maximum initial
5 milliohms maximum average increase
10 milliohms maximum individual increase
Low level contact resistance, compliant pin: 1 milliohm maximum initial
1 milliohm maximum change
Insulation resistance: 1000 megohms minimum
Withstanding voltage: 1 minute hold with no breakdown or flashover
Temperature rise vs. current: 30°C maximum temperature at 1 Ampere load, single circuit in free air using thermography
Mechanical Vibration, sinusodial:
Mechanical Vibration: No discontunuities of 1 microsecond or longer duration
Mechanical Shock: No discontunuities of 1 microsecond or longer duration
Mating Force: 0.75 N [2.7 ozf] maximum per contact. Average for entire connector.
Unmating Force: 0.15 N [.57 ozf] minimum per contact. Average for entire connector.
Compliant pin insertion: 31 N [7 lbf] maximum per pin average
Compliant pin retention: 13.35 N [3 lbf] minimum

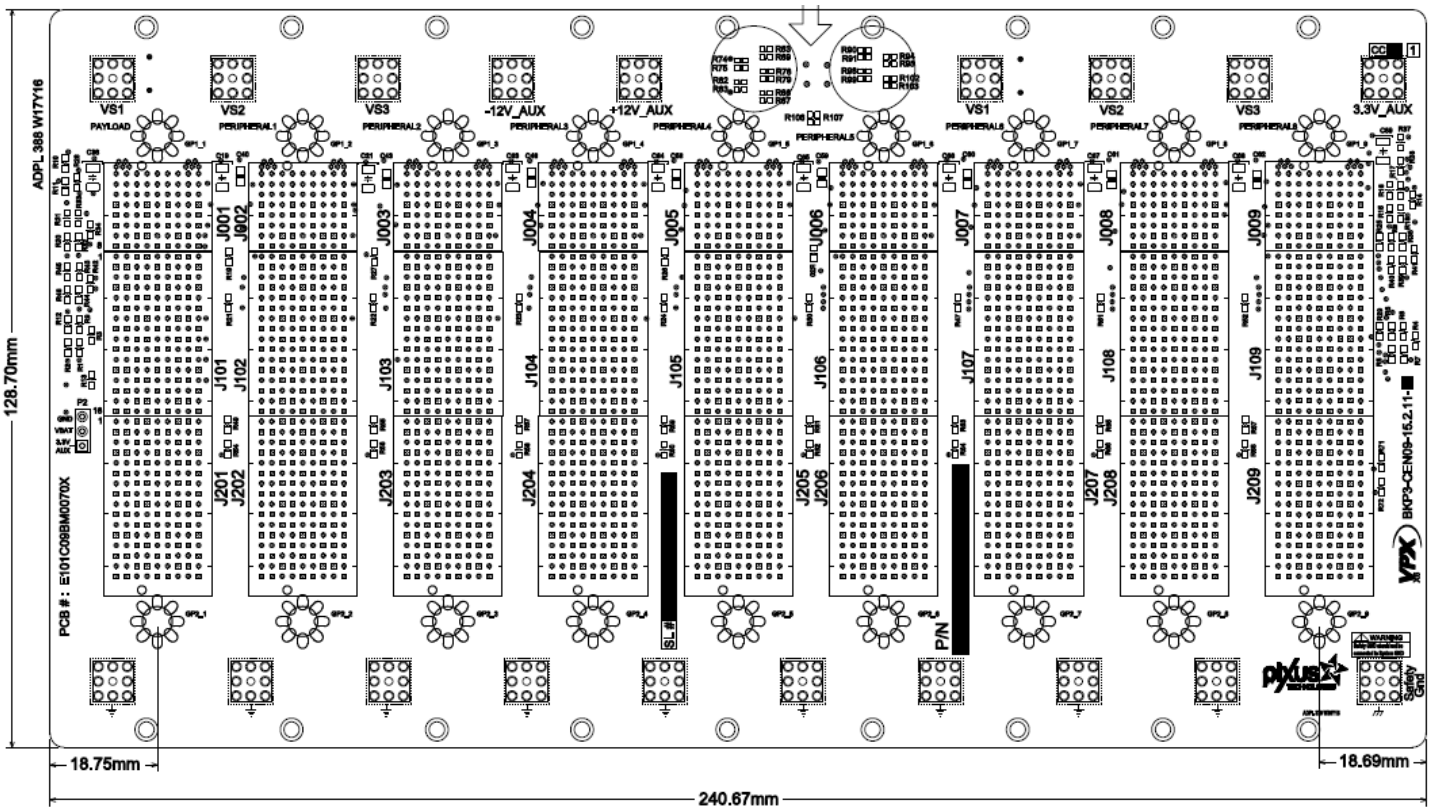
Signal Definitions:

Fat Pipe: A channel that is comprised of four links (4 Tx pairs + 4 Rx pairs) is now being referred to as a fat pipe or by use of the x4 nomenclature. 10Gbps capable 10GBase-KX4, 10GBase-BX4, 10GBase-T, PCIe-x4, sRIO-x4, Infiniband-x4

Thin Pipe: A channel that is comprised of two links (2 Tx pairs + 2 Rx pairs) is now being referred to as a thin pipe or by use of the x2 nomenclature. 5Gbps capable 10/100/1000Base-T, 1000Base-BX, PCIe-x2, sRIO-x2, Infiniband-x2

Ultra-thin Pipe: A channel that is comprised of one link (1 Tx pair + 1 Rx pair) is now being referred to as an ultra-thin pipe or by use of the x1 nomenclature. 10GBase-KR, IGBase-KX, PCIe-x1, sRIO-x1, Infiniband-x1a

3U Drawing—9-Slot Example with 1.0” Pitch



Ordering Options
VPX30=3U OpenVPX Backplane

VPX30-AB-CC-DFGHI-J

AB = VPX Slots

= 02-18

CC = Profile Topology

AA = CEN03-15.2.9
AB = CEN06-15.2.10
AC = CEN07-15.2.3
AD = CEN12-15.2.6
BA = DIS05-15.2.13

BB = DIS06-15.2.7
BC = DIS06-15.2.14
BD = DIS02-15.2.8
BE = CEN09-15.2.17
XX = Other

D = Slot Pitch

0 = 0.8”
1 = 1.0” (most common size)
2 = Custom

F = Voltage

1 = 5V, 12V (6U Only) and +/- 12V AUX, 3.3V AUX
2 = 3.3V, 5V, 12V (3U Only) and +/- 12V AUX, 3.3V AUX
3 = Other

G = Rear IO

A = Full rear IO connectors
X = No rear IO connectors
C = Partially loaded or custom

H = Data Rate

1 = Data plane 3.125 Gbaud
3 = 6.25 Gbaud
5 = 10 Gbaud (for 40G systems)
2 = 5.0 Gbaud
4 = 8.0 Gbaud (PCIe Gen3)
6 = Other

I = Power Interface

1 = M4 threaded stud
2 = 1 x VITA 62 PSU interface
3 = Other

J = Conformal Coating

0 = None
1 = Humiseal 1A33 Polyurethane
2 = Humiseal 1B31 Acrylic